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Characterization of ion implanted antimony

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CHARACTERIZATION OF ION IMPLANTED ANTIMONY

by

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FOREWORD

The experimental work described in this thesis was undertaken as a development project during my assignment as a process engineer in the Device Technology Lab of the Electronic Research Laboratories, Eastman Kodak Company. This facilitated the use of modern semiconductor processing and testing equipment and provided me with a number of well defined goals in the form of actual device applications. This was an enjoyable experience for me and, I hope, a useful project for my employer.

I wish to acknowledge the technical guidance of Prof. R. Turkman, Rochester Institute of Technology, during the past three years. In addition, I received a great deal of encouragement and support from many employees of Eastman Kodak Company; an incomplete list is: Mr. M. DeMay, Mr. M. Guidash, Mr. J. Hach, Mr. J. Hoover, Dr. J. Lavine, Dr. S. T. Lee (SIMS Analysis), Mr. J. Russell, Mr. A. Scribani and Dr. J. Taylor. I am also indebted to Mr. K. Chasey, Varian SEG, Inc., for assistance with ion implantation equipment. Finally, I am especially grateful for the patience of my wife, Judy.

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ABSTRACT

Ion implanted antimony (^{121}Sb) is characterized as an n-type dopant in single crystal (100) oriented silicon. The required implantation equipment and critical parameters are discussed. The experimental procedures used in this study are presented along with the resulting data on dopant distribution and crystal damage annealing.

The tradeoffs between antimony and arsenic, the more commonly used heavy n-type dopant, are examined from both a process and a device perspective. The context of this comparison is in applications that require a heavily doped layer beneath a thin deposit of epitaxial silicon. Results of a specific buried layer process characterization are included.

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x Vertical distance into the substrate measured from the surface.

$n(x)$ Density of impurity atoms as a function of vertical distance.

$\emptyset$ Ion dose; the number of implanted ions per unit area.

R_p Projected range; the average distance of vertical penetration into the substrate by implanted ions.

ΔR_p Projected standard deviation (vertical straggle); the statistical fluctuation in R_p.

ΔR_l Lateral standard deviation (lateral straggle); the statistical fluctuation in the lateral penetration of the substrate by implanted ions.

q_e Magnitude of the charge of an electron.

m Mass of an ion.

V_x Ion source extraction voltage.

h Charge state of an ion (1,2,3,...)

r Radius of curvature of the beamline within the analyzer.

B Magnetic field strength of the analyzer.

E_f Final ion energy.

V_a Voltage drop across the accelerating tube.

I_b Ion beam current.

A Target area over which the ion beam is scanned.

R_s Sheet resistance.

D Diffusivity.

D_N Diffusivity in a nonoxidizing atmosphere.

D_i^0 Intrinsic diffusion coefficient associated with neutral vacancy interactions.

D_i^- Intrinsic diffusion coefficient associated with negative vacancy interactions.

n Extrinsic carrier concentration.

n_i Intrinsic carrier concentration.

$[Si_I]_i$ Concentration of Si interstitials in a nonoxidizing ambient.

$[Si_I]$ Concentration of Si interstitials in an oxidizing ambient.

D_0^0 Pre-exponential factor associated with D_i^0.

D_0^- Pre-exponential factor associated with D_i^-.

Q_i^0 Activation energy associated with D_i^0.

Q_i^- Activation energy associated with D_i^-.

I. INTRODUCTION

The various microelectronic process technologies used in the fabrication of monolithic integrated circuits can be classified into three main groups:

1.) Bipolar technology.

2.) MESFET (metal-semiconductor field effect transistor) technology.

3.) MOSFET (metal-oxide-semiconductor field effect transistor) technology.

Each of these technologies relies upon successive iterations of a planar processing sequence to produce devices on semiconducting substrates, usually in wafer form. A block diagram of the "generic" planar process sequence is shown in Figure 1. The details of each element of this sequence may vary considerably between the iterations of a given process technology, but the overall form remains unchanged. As depicted in the block diagram, a doping process is not always used in each iteration. (The deposition and patterning of an aluminum interconnect layer is an example of this.)

"GENERIC" PLANAR PROCESS SEQUENCE

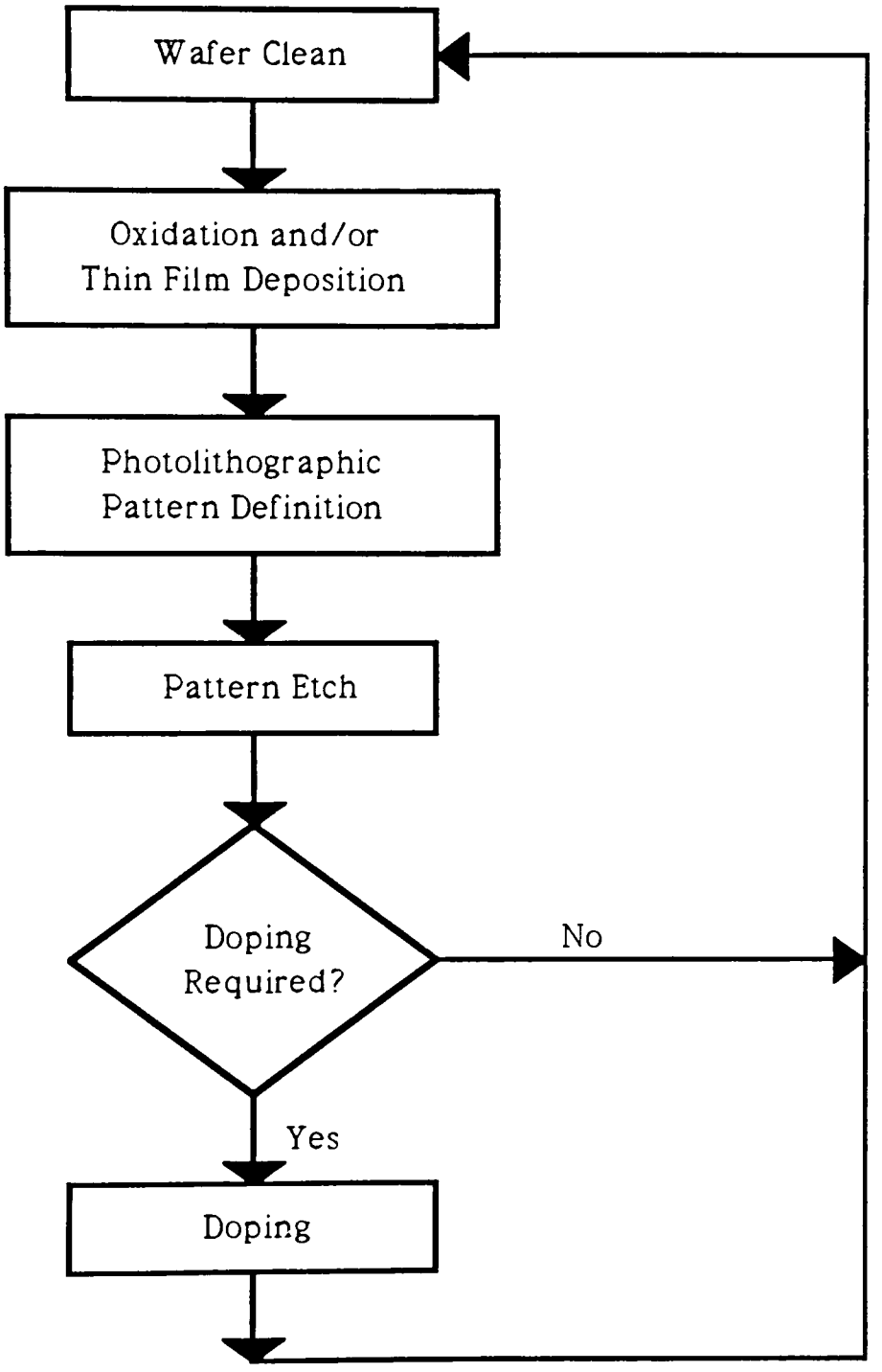

Figure 1

One feature of the planar process is the ability to modify the electrical properties of select regions of the semiconducting substrate. This is achieved by the introduction of substitutional dopants into the substrate lattice. Precise control of the three-dimensional distribution of dopant atoms is a key to successful device fabrication. The lateral dopant distribution is determined primarily by the photolithographic patterning and etching processes, while the vertical distribution depends upon the particular doping process used and any subsequent high temperature exposure.

The objective of this work is to characterize a specific doping process used in the fabrication of some silicon based microelectronic devices. Namely, the use of ion implanted antimony (^{121}Sb) as an n-type dopant is examined, emphasizing applications requiring a heavily doped buried layer structure.

A generalized discussion of the role of ion implantation is followed by a review of the technical literature on Sb implantation and device applications. Next, the engineering of an implanted Sb buried layer process is considered. The experimental procedures are described in

detail, including post-implantation annealing and wafer evaluation techniques. By way of comparison with arsenic (^{75}As), the more common heavy n-type dopant, the range statistics and annealing properties of Sb are presented.

II. ION IMPLANTATION AND MICROELECTRONICS

Ion implantation is the technique by which an energetic beam of ionized atoms is directed upon a solid target, resulting in the penetration of the target by the incident atoms. The range of energies encountered in most applications are such that the incident ions are able to penetrate beyond the near surface region (of the order of 50 Å) before coming to rest, without altering the structure of the nuclei of the target atoms.[1]

Ion implantation as applied to microelectronic device fabrication is the technique of choice for doping semiconductor wafers.[2] The common range of ion energies in contemporary processes is 5 to 500 keV. The number of implanted atoms per unit area of the target wafer, the dose, is usually between 10^{11} and 10^{17} atoms/cm^2. The energy and dose are the two fundamental parameters used to specify any ion implantation doping process.

As an individual implanted ion propagates into the target wafer, it loses energy via a multitude of scattering interactions with the

electrons and nuclei of the target atoms. This fact, coupled with the large absolute density of incident ions, mandates the use of statistics to predict adequately the final distribution of implanted atoms. The most elementary treatment of this problem results in a Gaussian distribution function of the form

$$n(x) = \{\emptyset / [\sqrt{(2\pi)}\Delta R_p]\} \exp \{-0.5[(x - R_p) / \Delta R_p]^2\} \qquad (1)$$

where x is the vertical distance into the target wafer, $\emptyset$ is the dose, R_p is the projected range (the average normal penetration depth) and ΔR_p is the projected standard deviation (vertical straggle).[3]

In the absence of crystallographic channeling effects, the Gaussian distribution function is a reasonable approximation near the peak of actual dopant profiles. However, because of the dependence of momentum transfer between implanted atoms and target atoms on their relative masses, forward or backscattering of the implanted atoms can occur.[4] This results in a skewed dopant profile which is not predicted by the Gaussian function. Three and four moment distribution functions have been fitted to experimental data permitting more accurate process modeling.[5,6]

The utility of these more complex distribution functions becomes significant in situations where the redistribution of implanted atoms due to any subsequent high temperature processing is negligible. Thus, if the cumulative $\sqrt{(Dt)}$ product of the processing which follows a given implantation step is much greater than ΔR_p, then the Gaussian function is sufficient for most process engineering problems. This is usually the case in Si processing. The range statistics of the shallow level impurities of Si and GaAs have been extensively studied and are widely published.

There are many desirable features of ion implantation as a doping technique as compared with furnace predeposition. The most important are listed below:

1. Cleanliness: Ion implantation takes place in a high vacuum environment, with the pressure typically 1×10^{-6} torr or lower. All implanters utilize some form of magnetic mass separation to produce a chemically pure beam of ions.
2. Flexibility: Magnetic mass separation means that one implanter can be used for many dopants. The wide range of achievable ion doses frees the process engineer from the

thermodynamic constraints encountered in furnace predeposition. Since most implanters are designed to maintain low wafer temperatures (<100°C), a host of alternate materials are useful as masks for selective doping.

3. Profile Control: The ability to adjust the ion energy enables control of the implanted dopant profile shape to a degree which is not possible by any other selective doping process.
4. Uniformity: Typical three-sigma dose uniformity specifications of a commercially available implanter are[7]
   (a) Within a wafer: $3s < 3.75\%$
   (b) Wafer to wafer, day to day: $3s < 1.50\%$

There are also several drawbacks to ion implantation:

1. Cost: Ion implanters range in price from about $400,000 for a medium current machine (I_{max} = 1 mA) up to $2,000,000 for a high current machine (I_{max} = 10 mA).
2. Complexity: An ion implanter is a complicated ensemble of high vacuum components, sensitive electrical subsystems and a wafer transport mechanism. Maintenance requirements are

significant, with downtimes of 25% not unusual.

3. Crystal Damage: An unavoidable by-product of ion implantation into single crystal material is disruption of the lattice. High temperature annealing is required to repair the damage. This requirement conflicts with the trend in VLSI device fabrication toward lower thermal budgets to achieve smaller vertical and lateral structures.

The basic layout of most commercial ion implanters is similar. The schematic of a common medium current unit[8] is shown in Figure 2. The flight path of the dopant atoms is traced below:

1. A D.C. gas plasma is used to ionize dopant atoms in the source. The internal pressure of the source is about 10^{-3} torr.*
2. Ions are extracted through an aperture in the source, at an energy between 5 and 25 keV, into the beamline.
3. The 90° bend in the beamline is nested within the uniform field of the analyzer magnet. The field strength is adjusted so that the trajectory of ions of the desired charge-to-mass ratio has the same radius of curvature as the bend in the beamline.

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* A more detailed discussion of sources is in Chapter III.

VARIAN/EXTRION CF4/DF4 ION IMPLANTER

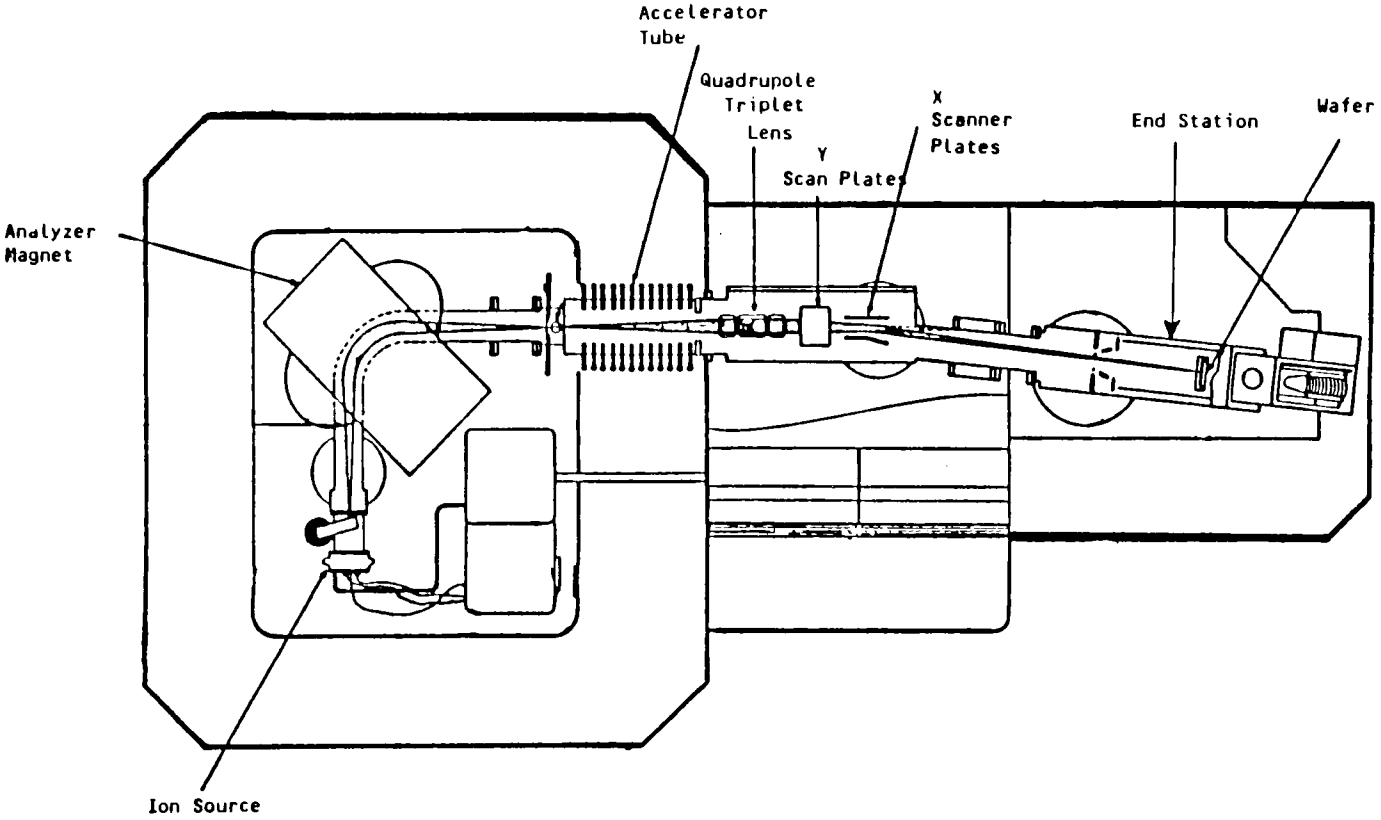

Figure 2

Reference: Varian/Extrion DF4/CF4 specification booklet.

The charge-to-mass ratio is given by*

$$q_e/m = 2V_x / (hr^2B^2) \qquad (2)$$

where h is the charge state of the ion , q_e is the magnitude of the charge of an electron, m is the mass of the ion, V_x is the extraction voltage applied to the ion source, r is the radius of curvature of the beamline and B is the field strength of the analyzer magnet.

4. After being filtered by the analyzer magnet, the ion beam passes through a variable aperture to adjust the current level. The beam is then accelerated across the high voltage tube, which boosts the energy of the ions to the final value, E_f.

$$E_f = hq_e(V_x + V_a) \qquad (3)$$

V_a is the voltage drop across the accelerator tube. The high voltage end of the beamline between the source and the accelerator tube is maintained at a pressure of approximately 10^{-4} torr, corresponding to a mean free path of 50 cm.

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* See Appendix 1 for a derivation.

5. The next section of the beamline contains an electric quadrupole triplet lens for beam focusing plus vertical and horizontal scan plates to raster the beam uniformly across the target wafer. One key feature of the scan system is a D.C. offset voltage applied between the horizontal plates to deflect the beam by about 7°. This eliminates any neutral atoms from the beam that result from charge exchange as ions traverse the high voltage end of the beamline. Charge exchange is not an issue past the accelerator tube because the pressure is kept below 5×10^{-6} torr, which corresponds to a mean free path of greater than 10,000 cm.

6. The scanned ion beam enters the end station and impacts the target wafer. The wafer resides within a Faraday cage to suppress any secondary electron emission, which would otherwise lead to significant dose errors. The electron current which is supplied to the wafer to neutralize the implanted ions is integrated to determine the dose. The relationship between the dose, the scanned area, A, and the beam current, I_b, is

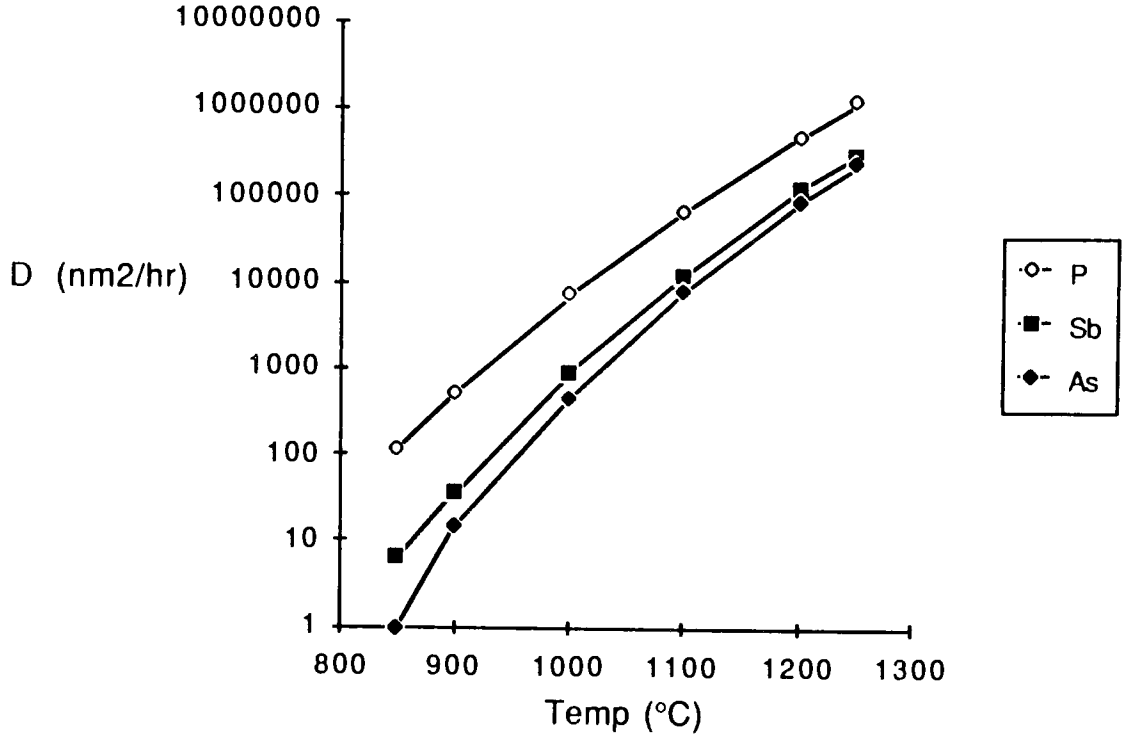
$$\phi = (\int I_b dt)/(nq_e A) \qquad (4)$$

III. ANTIMONY IMPLANTATION INTO SILICON

Many microelectronic devices require localized regions doped with an n-type impurity that diffuses slowly in the host lattice. In the case of Si, the n-type dopants that fufill this requirement are As and Sb; see Figure 3. These two materials can be chemically predeposited in a diffusion furnace or ion implanted.

Before engaging in consideration of Sb ion implantation, there should be some mention of the fact that a materials problem originally caused workers in the field to seek an alternative to chemical predeposition of As and Sb. This problem, which is common to both As and Sb when chemically predeposited on Si, is the formation of impurity rich defects called "rosettes". The elimination of As induced rosettes was one goal of R. A. Moline's work on ion implanted As to form heavily doped layers beneath epitaxial Si.[9] Similarly, G. M. Oleszek has characterized a technique for the formation of heavily doped, rosette free, Sb buried layers using a low current (I_{max}= 25 μA) implanter.[10]

Intrinsic Diffusivities in Si



Reference: Technology Associates, Semiconductor Technology Handbook, p. 6.2, 1985.

Figure 3

Ion implantation of Sb into Si has been fundamentally characterized in the range of energies between 10 keV and 60 keV by W.K. Chu.[11] Using SIMS analysis, the $\Delta R_p/R_p$ ratio was found to be constant at about 0.3 (± 20%). (The determination of higher moments is reportedly too sensitive to experimental noise for an accurate extraction by this method.) For process modeling, a modified LSS* nuclear scattering potential was fitted to the data.

Sb implantation in the energy range of 30 keV to 120 keV has been studied by E. Guerrero.[12] SIMS and RBS measurements were used to determine the dopant profiles before and after annealing. Sb was found to precipitate at concentrations above $6 \times 10^{19}/cm^3$ if the annealing temperature exceeded 800°C. For samples with high implant doses ($Ø = 3 \times 10^{15}/cm^2$), an anomalously high oxidation rate (2X) was observed.

Most ion implantation into Si wafers is done through a thin layer of surface oxide to minimize crystal channeling effects and to protect

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*LSS: Lindhard, Scharff and Schiott, authors of Reference 3, the original paper on ion implantation range theory.

the underlying Si from contamination by forward scattered impurities (from either the implanter apertures or masking layers on the wafer). The behavior of implanted As and Sb in the vicinity of the Si-SiO_2 interface was analyzed be G. A. Sai-Halasz.[13] Moderate dose implants ($5 \times 10^{14}/cm^2$) were done at low energies (40 to 50 keV) through a thin oxide layer (100 Å). RBS data indicated that for annealing temperatures of 900 to 1000°C, both dopants have an essentially unity sticking coefficient at the Si-SiO_2 interface until $2 \times 10^{14}/cm^2$ is segregated. This trapped dopant is electrically inactive.

A more rigorous investigation of the activation properties of ion implanted Sb was published by A. Nylandsted Larsen.[14] Using RBS, Hall-effect measurements and Mossbauer spectroscopy, the maximum electrically active Sb concentration (incorporated on substitutional sites) was found to be $4.5 \times 10^{20}/cm^3$ for 700°C annealing. With further annealing, this "supersaturated solution" can be reduced. The Sb goes out of solution into Sb-Si vacancy complexes at low doses and low annealing temperatures, and into Sb precipitates at high doses and high temperatures.

The effect of the furnace tube atmosphere on the diffusivity of Sb in Si has been studied by S. Mizuo.[15] Spreading resistance probe (SRP) and angle lap-and-stain measurements have shown that Sb diffusion is retarded in an oxidizing atmosphere relative to a non-oxidizing atmosphere. At 1100°C, the diffusion coefficient in dry O_2 is 40 to 50% of the value obtained in N_2, depending upon the oxidation time. This behavior, which is unique among Si dopants, indicates that Sb diffuses with vacancies exclusively.

Beyond the basic Sb implantation and annealing studies, a number of papers have been published on specific applications. Many of these are concerned with devices that require a heavily doped n-type layer beneath a thin (2 to 20 μm) deposit of epitaxial silicon. Vertical npn bipolar and n-well CMOS devices are the most commonly cited applications. In the case of the vertical npn bipolar transistor, the use of a heavily doped buried collector layer reduces the series collector resistance, permitting a lower collector-to-emitter voltage in saturation mode. The buried layer also minimizes the current gain of the parasitic pnp transistor formed by the base, collector and

substrate.* See Figure 4.[16]

The benefit of a buried layer in CMOS devices lies in latch-up immunity.[17] If the n-well is diffused down through a p-type epi-layer into a heavily doped n-type buried layer, a retrograde n-well profile is achieved. By degrading the gain of the parasitic pnp transistor formed by the p^+ source/drain, n-well and substrate, latch-up immunity is improved.* See Figure 5.

J. P. Gailliard investigated heavily doped buried layers in a bipolar process using ion implanted Sb.[18] He considered the role of substrate crystal orientation on the effectiveness of post-implant furnace annealing. TEM study indicated that residual defects are more difficult to eliminate in (111) Si than (100) Si. During recrystalization of the implant generated amorphous region, the formation of microtwins was observed only in (111) Si. The

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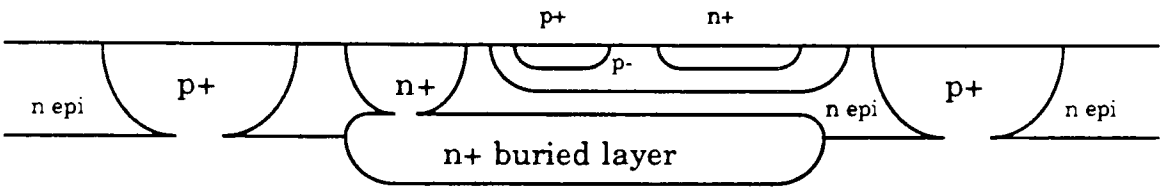
* The parasitic emitter injection efficiency is reduced due to the increased base Gummel number. Furthermore, the transport factor of the parasitic base is degraded by the built-in electric field associated with the retrograde doping profile and the increased base width.

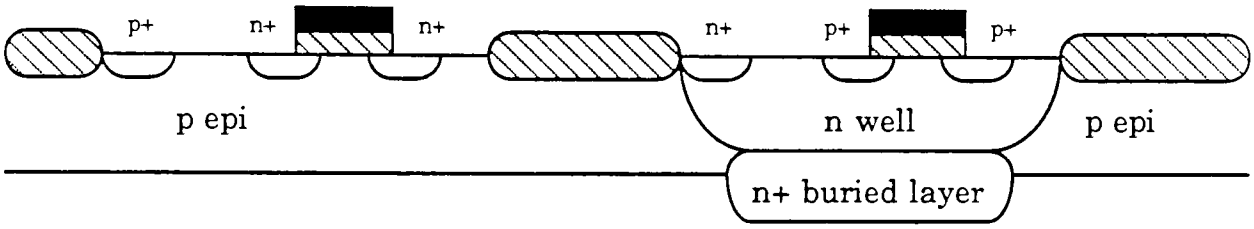
Vertical NPN Bipolar Transistor



p - substrate

Figure 4

N Well CMOS Structure



p+ substrate

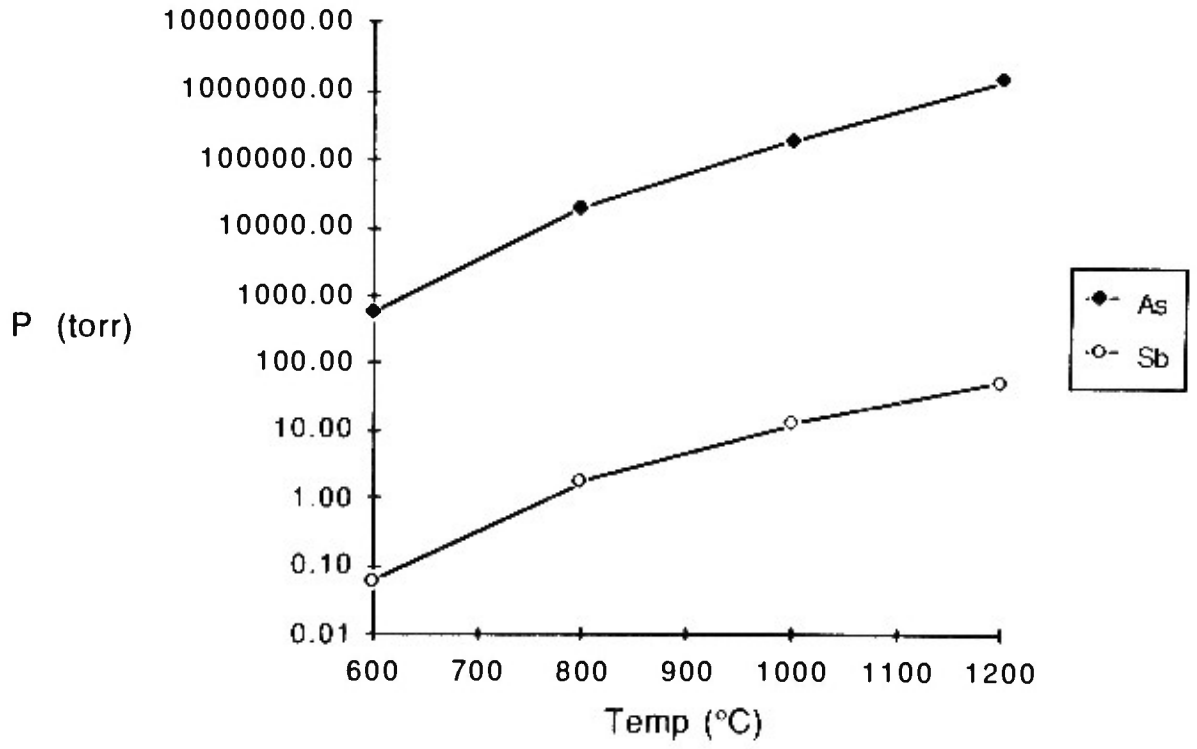
Figure 5

microtwins are apparently stable at annealing temperatures of up to 1200°C, and lead to defective epi-layers.

An unexpected benefit of buried layer structures is the elimination of epi-layer defects via extrinsic gettering. G. A. Rozgonyi has published results of a bipolar process gettering study.[19] This demonstrated the effective denuding of epitaxial defects (primarily stacking faults) which were within 100 µm of an implanted Sb buried collector island.

M. L. Hammond has considered the problem of autodoping during epitaxial growth with respect to localized confinement of buried layers of As and Sb.[20] Autodoping is the redistribution of dopant near the original wafer surface during epi-layer deposition due to evolution of the dopant into the epi-reactor atmosphere. This effect, which depends upon the vapor pressure of the dopant, can result in unwanted spreading of the localized buried layer islands in the vertical and lateral directions as well as cross contamination of adjacent wafers in a batch reactor. The vapor pressures of As and Sb are shown in Figure 6. The lower vapor pressure of Sb, especially at

Vapor Pressures of Sb and As



Reference: A. N. Nesmeyanov, Vapor Pressure of the Chemical Elements, pp. 292-299, edited by R. Gray, Elsevier, Amsterdam, 1963.

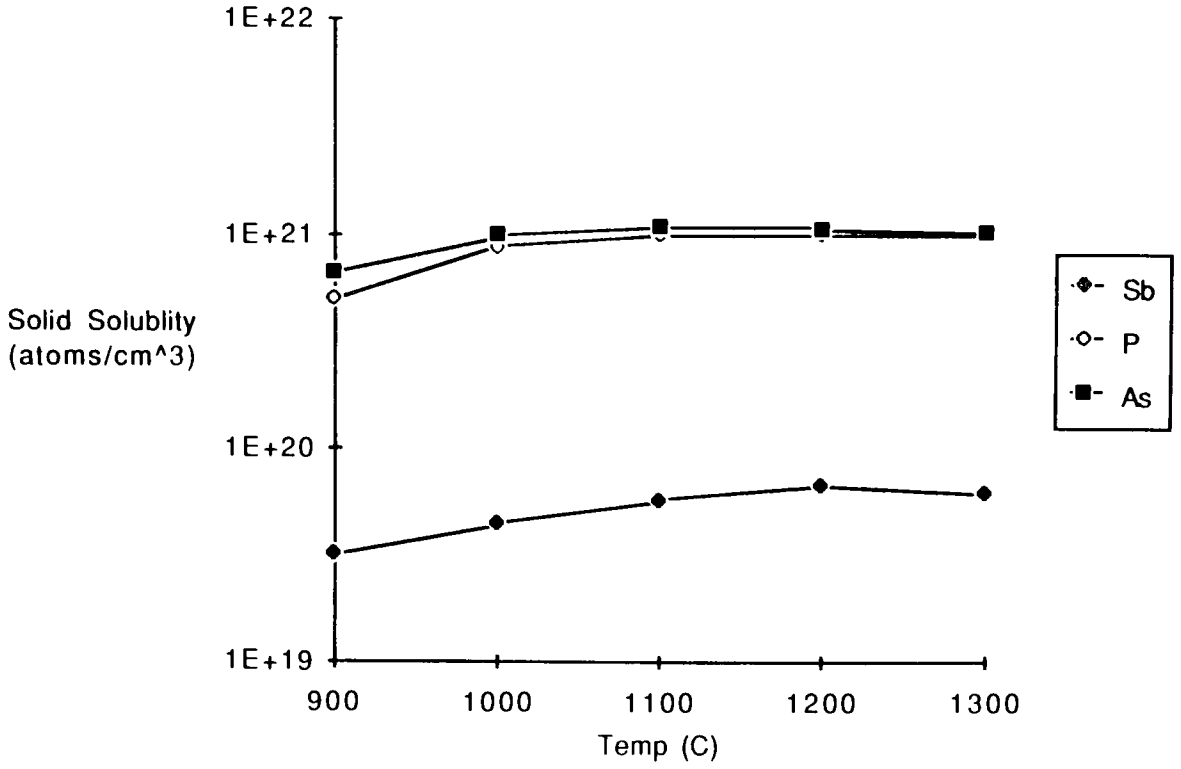
Figure 6

typical epi-reactor temperatures (1050°C to 1200°C), is the overriding reason for its use as a buried layer dopant.

If a buried layer with a very high peak doping concentration (greater than $5 \times 10^{19}/cm^3$) is necessary, Sb is no longer a viable alternative to As because of its lower solid solubility in Si. The solid solubilities of the common n-type dopants are shown in Figure 7 and their tetrahedral bonding radii are listed in Table 1.

Sb has found other applications in Si devices beyond buried layer structures. Because of the large atomic mass of Sb relative to Si (121:28), it can very effectively amorphize single crystal Si under the proper implantation conditions. A. Schmitt has evaluated Sb implantation as a preamorphization technique.[21] After implanting Sb at a dose of $1 \times 10^{14}/cm^2$, phosphorus was implanted into the amorphous Si layer at a high dose, $3 \times 10^{15}/cm^2$. The energies of the two implants were chosen such that the profile was completely contained within the amorphous layer. Normally, P implanted at this dose level without any preamorphization results in dislocation loops in the Si after annealing. However, the moderate dose Sb

Solid Solubilities in Si



Reference: Technology Associates, Semiconductor Technology Handbook, p. 6.1, 1985.

Figure 7

Table 1: Atomic Masses, Tetrahedral Bonding Radii and Lattice Misfit Factors of n-Type Dopants in Si

Dopant	Sb	As	P
Atomic Mass of Most Abundant Isotope (amu)	121.8	74.9	31.0
Tetrahedral Bonding Radius (Å)	1.36	1.18	1.10
Lattice Misfit Factor	0.153	0.0	0.068

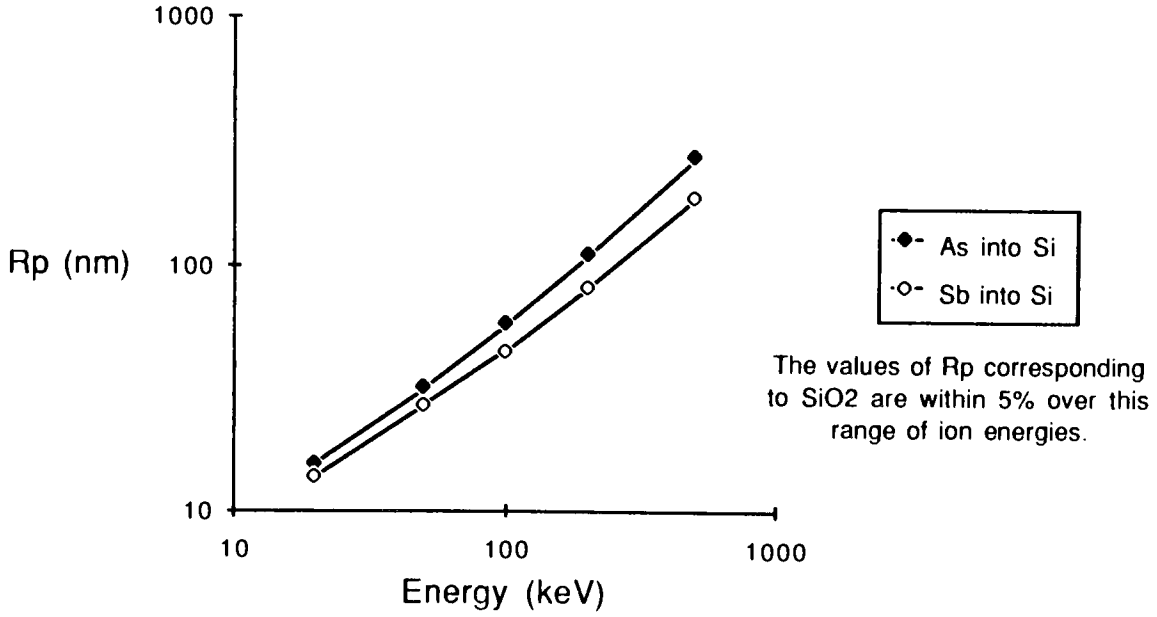
Reference: S. K. Ghandhi, The Theory and Practice of Microelectronics, p. 6, Wiley, New York, 1968.

preamorphization implant enables defect free recrystalization of the heavily doped layer.

One approach to fabricating reliable short channel (1 μm) NMOSFETs requires the use of a source/drain extension implant. Known as a low-doped-drain (LDD), this places a shallow, lightly doped lateral extension of the usual n^+ source/drain regions under the edge of the gate.[22,23] G. A. Sai-Halasz has outlined a method of fabricating the necessary shallow junction (100 Å) extensions with moderately low sheet resistance values (200 Ω/□ to 500 Ω/□).[24,25] Ion implanted Sb is chosen as the LDD dopant because of its reduced vertical and lateral straggle for a given projected range as compared with As. See Figures 8, 9 and 10.

The comparatively low values of R_p and ΔR_p for ion implanted Sb make it useful for lowering the Schottky barrier heights of metal-Si diodes. W. K. Chu has published results on TiW-Si diodes, with a 100 mV to 150 mV barrier height lowering using shallow Sb implants prior to metal deposition.[26] S. Ashok has reported similar results on Al-Si diodes.[27]

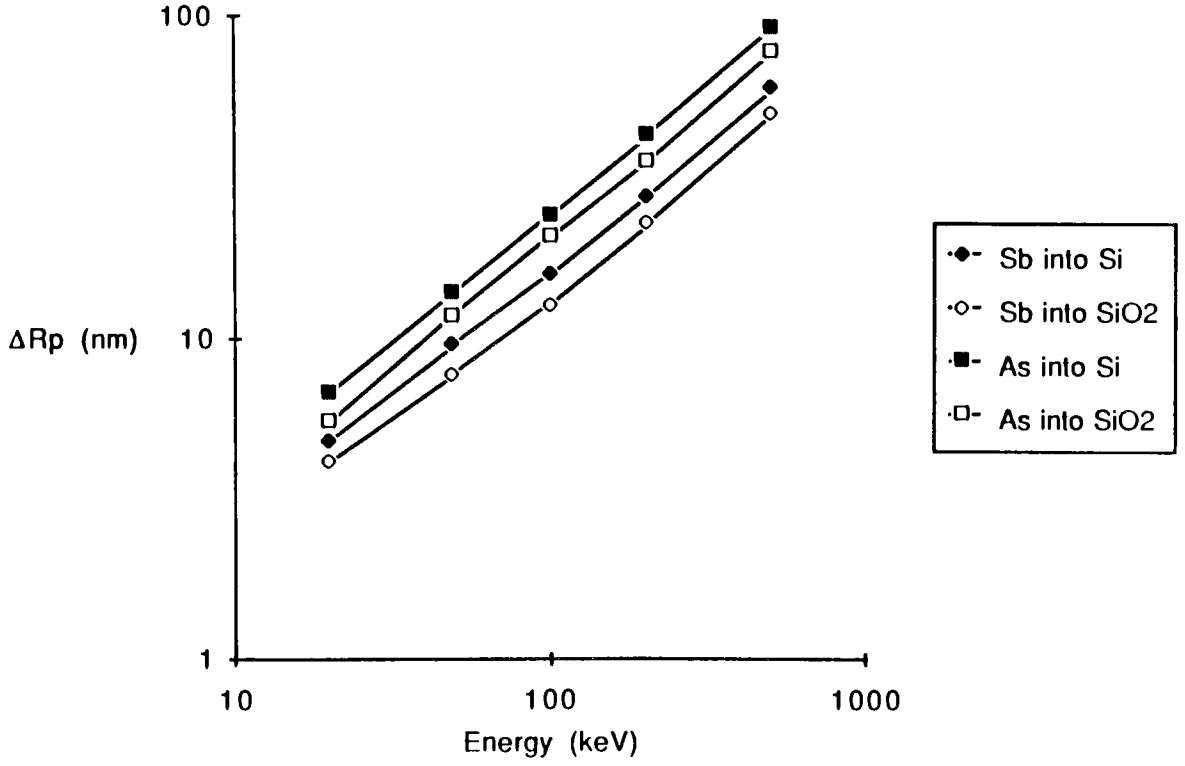
Projected Range (Rp) of Sb and As



Reference: Technology Associates, Semiconductor Technology Handbook, p. 7.1, 1985.

Figure 8

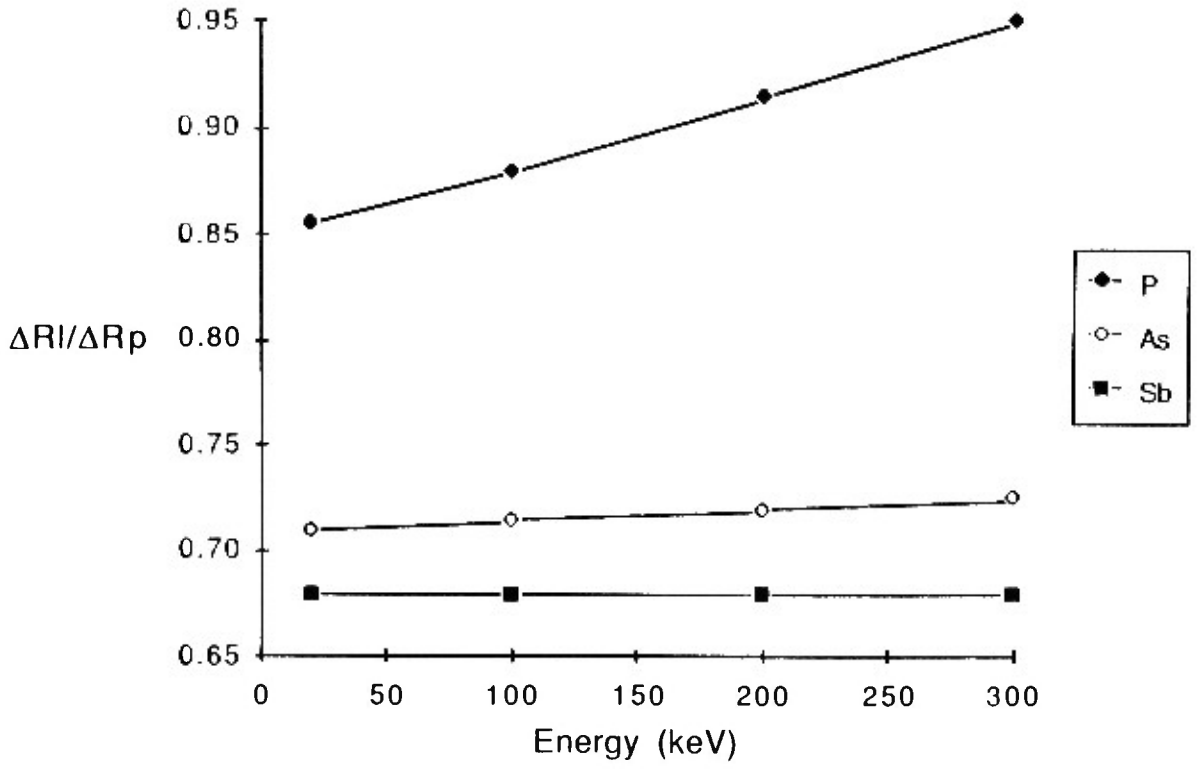
Projected Std. Dev. (ΔRp) of Sb and As



Reference: Technolgy Associates, Semiconductor Technology Handbook, p. 7.2, 1985.

Figure 9

Ratio of Lateral and Vertical Straggle (ΔRl/ΔRp) in Si



Reference: Technology Associates, Semiconductor Technology Handbook, p. 7.5, 1985.

Figure 10

There are two key equipment issues which must be addressed in order to implant Sb: the method of ionizing Sb atoms and the mass separation of Sb ions. Since these are equipment specific issues, the remainder of this discussion is based on a widely installed medium current implanter, the Varian/Extrion Model 200 CF4, which was the machine available for this work.

The ion source system used in the CF4 implanter is a hot cathode magnetron unit; see Figure 11. The cathode is a tungsten filament through which a high current (150 A) is forced, causing thermionic emission of electrons. The electrons are subjected to an electrostatic force due to the potential difference between the cathode and anode (usually 60 V). As the electrons drift across the arc chamber, their path is deflected by magnetic forces due to the axial field of the source magnet and the circular field induced by the filament current. (This serves to enhance their ionization efficiency by increasing their path length in the arc chamber.)

As a source gas is bled into the arc chamber, increasing the pressure to about 10^{-3} torr, a plasma is established. If B, P, or As ions are

Vaporizer Equipped Ion Source

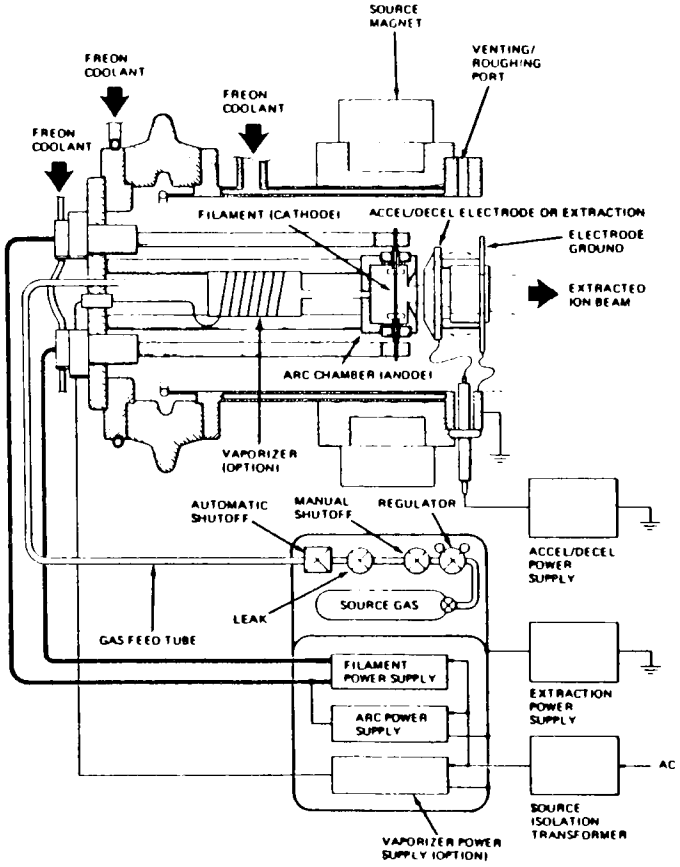


Figure 11

Reference: Varian/Extrion DF4 specification booklet.

needed, a direct gas fed source is possible using BF_3, PH_3 or AsH_3, respectively. If a gaseous form of the desired element is not available, a more complicated approach is necessary to generate ions. In the case of a low vapor pressure solid (such as Sb), a resistively heated oven can vaporize the solid and direct the vapor into the arc chamber. An inert gas such as Ar must be used to maintain a plasma.

A photograph of the vaporizer oven assembly used in the CF4 implanter is shown in Figure 12. A graphite crucible containing the desired solid source material is located inside a boron nitride tube, around which tungsten heater wire is wound. The crucible temperature is monitored be a type K thermocouple inserted into the side of the BN tube. The heater and thermocouple are in a closed loop temperature control system with regulation to 1°C over the range of 160°C to 800°C. The vaporizer assembly fits into the center of the standard CF4 gas fed ion source. A standard ion source and a vaporizer equipped source are shown in Figure 13.

Positively charged ions are extracted from the source plasma through a vertical slit in the front surface of the arc chamber. The potential

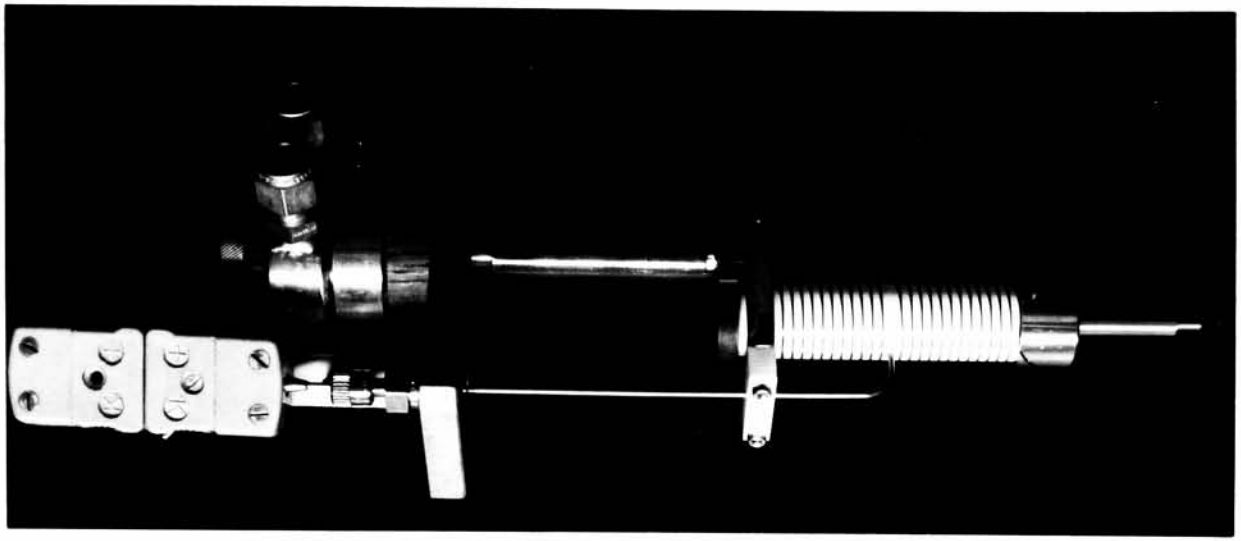


Figure 12

Varian/Extrion CF4 solid source vaporizer core.

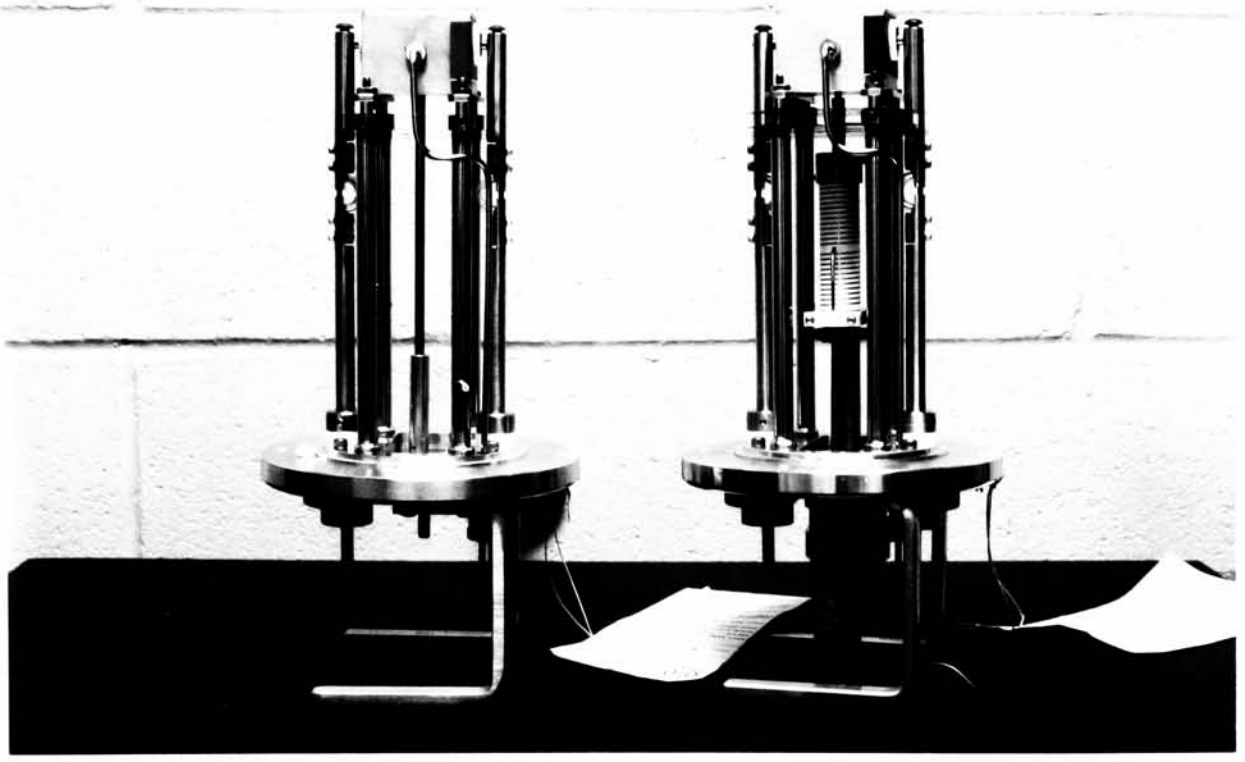


Figure 13

A standard CF4 gas fed ion source (left) and a vaporizer equipped source (right).

difference between the arc chamber and the extraction electrode is the extraction voltage, V_x.

The CF4 implanter used in this work is equipped with an analyzer magnet designed to mass separate singly charged ions from 1 amu* to 75 amu at the maximum extraction voltage, 25 kV. From equation 2, with the radius of curvature fixed and the magnetic field maximized, a reduction of the extraction voltage is necessary to extend the range of mass separation. However, a penalty is incurred since the ion beam current is strongly dependant on the extraction voltage. In Figure 14, empirical data from a CF4 implanter illustrates the tradeoff.

It is evident that the extraction voltage must be limited to 16 kV to analyze $^{121}Sb^+$. This results in a beam current degradation of nearly 50 % for $^{75}As^+$. The implication is that the maximum value of $^{121}Sb^+$ beam current achieved with V_x = 16 kV is only about half of what would be possible with a larger analyzer magnet and V_x = 25 kV.

---

*1 amu is defined as 1/12 of the mass of the ^{12}C atom;
1 amu = 1.66×10^{-27} kg.

Beam Current and Mass Separation vs. Extraction Voltage

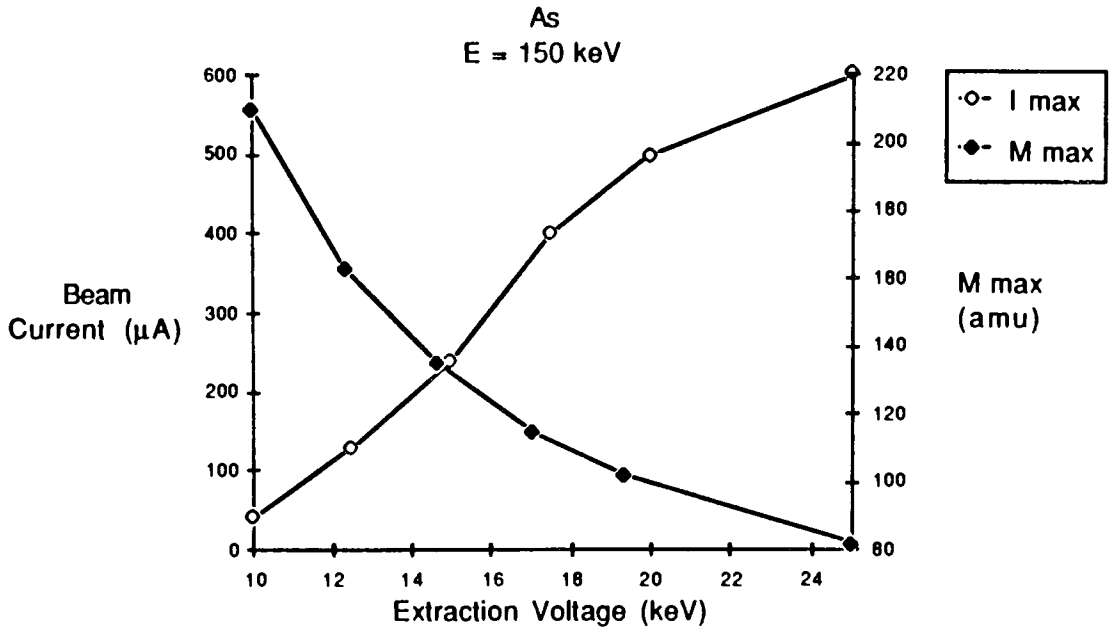


Figure 14

The excessive size and mass (4000 lb) of the analyzer make its replacement with a larger magnet prohibitive as long as the implanter's wafer throughput is acceptable at the reduced beam current.

Two isotopes of Sb exist: ^{121}Sb and ^{123}Sb. The naturally occurring isotope ratio is 57/43, respectively.[28] These facts permit unambiguous identification of the correct ion species when an implanter is tuned to implant Sb. The ^{121}Sb isotope yields the greater ion beam current due to its relative preponderance.

Given the availability of a suitable solid vaporizer ion source and the published information on implanted Sb range statistics and annealing properties, the development of a buried layer doping process should be a straightforward engineering exercise. The balance of this work is centered around the characterization of two device specific versions of an Sb buried layer process. Verification of the basic properties discussed in the literature are attempted along the way.

IV. EXPERIMENTAL PROCEDURE

The characterization of any ion implantation doping process is of necessity intimately tied to the subsequent furnace annealing process. Having defined the substrate properties (orientation and doping) and the required features of the implanted layer after annealing (dopant type, junction depth, peak concentration, sheet resistance, etc.), the experimental procedure is as follows.

1. Optimization of the ion source performance to provide a pure and stable supply of the desired dopant ions.
2. Verification of the correct ion species and their range statistics as implanted.
3. Determination of the annealing/diffusion properties of the implanted dopant.
4. Characterization of the implanted layers after diffusion. This requires the evaluation of sheet resistance vs. ion dose as well as measurement of the dopant distribution.
5. Final optimization of implantation and diffusion parameters for acceptable integration with subsequent processing.

In this thesis, 4-inch diameter 40-Ωcm boron doped (100) CZ wafers are used for all experiments. Wafers are tilted 7° off normal incidence with respect to the ion beam during Sb implantation.*

Two versions of an Sb buried layer process are required. The target features of each version are listed in Table 2. Irvin's curves[29] indicate that these combinations of junction depth, sheet resistance and peak concentration are achievable in the specified background concentration (for 40 Ωcm p-type Si, $N_{BC} \approx 3 \times 10^{14} / cm^3$).

Optimization of a vaporizer equipped source for the ionization of Sb is a fairly straightforward task. Baseline source operating parameters are provided by the implanter manufacturer, Varian/Extrion. The final result of this effort takes the form of a mass spectrum of the ion source output, which is obtained by plotting beam current vs. analyzer magnetic field. This spectrum qualifies the purity of the solid Sb source material and the carrier gas (Ar).

---

* This is generally the standard Si wafer orientation during ion implantation since axial channeling effects are minimized. Without a parallel beam scanning configuration, axial channeling cannot be eliminated.

Table 2: Target Features of Sb Implanted Layers After Drive-In

Feature	Version A	Version B
Implantation Screen Oxide Thickness (Å)	600	250
Junction Depth (μm)	5.00	1.75
Peak Concentration (atoms / cm3)	$< 5 \times 10^{19}$	$< 5 \times 10^{18}$
Sheet Resistance (ohms / square)	< 20	< 400
Post-Diffusion Oxide Thickness (Å)	> 4000	3000

The range statistics of implanted Sb in Si and SiO_2 are determined using SIMS analysis. Concurrence with the published data is sufficient verification of the implanter's high voltage calibration. SIMS also provides an independent identification of the implanted atoms and permits a crude evaluation of dose control.

An understanding of the annealing and diffusion properties of ion implanted Sb in Si is vital for successful process integration. An important parameter is the critical dose (ϕ_c) for the formation of an amorphous surface layer in single crystal Si. Generally, annealing of ion implantation damage can be characterized in terms of ϕ_c.

Isochronal furnace annealing and four point probe sheet resistance measurements have been used by B. L. Crowder to determine ϕ_c for As.[30] In this thesis, the values of ϕ_c corresponding to As and Sb are obtained using isochronal rapid thermal annealing (RTA)* and four point probe measurements.

---

* RTA is a useful tool for annealing a large number of samples under different conditions (i.e. temperatures and/or times).

The degree of oxidation retarded diffusion (ORD) of Sb is of special interest fundamentally because none of the other Si dopants exhibit this behavior. SRP measurements are used to characterize Sb ORD in Version B (see Table 2) layers diffused in either N_2 or dry O_2.* To facilitate accurate process simulation, any necessary adjustments of the SUPREM III default diffusion parameters are determined.[31] At this point, furnace diffusion schedules which are consistent (to 1st order) with the requirements listed in Table 2 can be formulated.

Electrical characterization of implanted Sb layers after diffusion requires the generation of sheet resistance vs. implantation dose and energy curves. The uniformity of the combined implantation and diffusion processes is easily evaluated with contour maps of sheet resistance data at the wafer level.

---

* It seems appropriate to mention here the importance of substantial oxide growth during buried layer diffusion in some applications. Assume that the buried layer implant is selectively masked by a thick initial oxide (> 5000Å) and the subsequent diffusion and oxidation process is performed without removal of the patterned initial oxide. It is clear that more Si is consumed in the buried layer regions than in the masked regions by this post-implant oxidation. Therefore, a step is formed on the Si surface around the perimeter of the buried layer islands. This step may be a useful alignment aid for subsequent photolithographic patterning.

The redistribution of buried layer dopant up into the epi-layer (autodoping) was discussed in Chapter III. This is the key issue in the integration of a buried layer sequence into a device fabrication process.

There are a limited number of process variables that can be altered to enhance the abruptness of the buried layer to epi-layer doping profile. In terms of the buried layer features, the peak concentration should be minimized (i.e. a deeper junction) to reduce autodoping.[32] In general, the collective Dt product of all high temperature process sequences after buried layer diffusion should be minimized.

The epi-layer deposition process itself offers some opportunity for the reduction of autodoping. The minimum reactor temperature and maximum deposition rate consistent with crystal quality requirements should be used. The enhanced gas diffusion rates encountered in low pressure epi-reactors offer some improvement in autodoping, especially with As buried layers.[33] In some applications, tailoring of the epi-layer doping profile during deposition to compensate for autodoping from the buried layer may be possible.

The autodoping problem is addressed in this work by comparing similarly implanted and diffused Sb and As "Version B" buried layers (see Table 2). The Sb buried layer structure is achieved by depositing an epi-layer in an atmospheric pressure reactor. The As buried layer structure is achieved by depositing a similar epi-layer in a reduced pressure reactor. With similar thermal cycles and identical deposition rates, this represents a "worst case" Sb autodoping scenario and a "best case" As autodoping scenario. SRP measurements are used to determine the doping profiles.

V. PROCESSING DETAILS AND RESULTS

The initial optimization of the solid vaporizer ion source is conducted at the lowest anticipated $^{121}Sb^{+}$ energy (50 keV). After charging the crucible with 10 grams of Sb shot (2 mm diameter, 5 nines purity), the source is pumped down to about 2×10^{-7} torr. As outlined in Chapter III, the extraction voltage is reduced to 16 kV, an Ar plasma is established in the arc chamber and then the vaporizer temperature is ramped up to 700°C at a rate of 10°C/minute.

At this point, the various source parameters (Ar flow, vaporizer temperature, filament current, source magnet current and arc current) are adjusted to maximize the Sb scanned beam current. As might be expected, the maximum current is obtained by stopping the flow of Ar, thereby sustaining the source plasma solely with Sb vapor. However, frequent discharging of the extraction voltage results. This is caused by undesired condensation of Sb vapor on the source insulators. If a moderate flow of Ar is restored, the condensation induced discharging ceases but the beam current decreases by about 13%. This tradeoff is necessary to ensure a

reliable and stable supply of Sb ions. The measured source parameter values are listed in Table 3.

The ion source mass spectrum is shown in Figure 15. The peaks corresponding to singly and doubly charged ^{40}Ar, ^{121}Sb and ^{123}Sb ions are labeled. The absence of any other significant peaks demonstrates the purity of the Sb and Ar and also verifies the integrity of the vacuum system.

As a final qualification of the vaporizer ion source performance, the effect of ion energy (i.e. accelerating voltage) on $^{121}Sb^+$ beam current is measured. The maximum current for energies in excess of 140 keV is 155 μA. See Figure 16. The maximum possible power dissipation during Sb implantation is 325 mW/cm^2 (E = 190 keV, I = 155 μA, A = 90.9 cm^2). The wafer temperature remains below 50°C on the Freon cooled platen at this power level.[34]

To determine the range statistics of ion implanted $^{121}Sb^+$, bare wafers and thermally oxidized (6000 Å) wafers are implanted with a dose of 1 x 10^{15}/cm^2. The Sb concentration profiles in Si and SiO_2

Table 3: Optimum Source Parameters For Sb Ionization

Ion Source Parameter	Value
Pressure (as measured at the source diffusion pump inlet)	8×10^{-6} torr
Vaporizer Temperature	780°C
Extraction Voltage	16 kV
Extraction Current	3.0 mA
Arc Voltage	60 V
Arc Current	1.0 A
Filament Current	150 A
Source Magnet Current	1.2 A

Ion Source Mass Spectrum

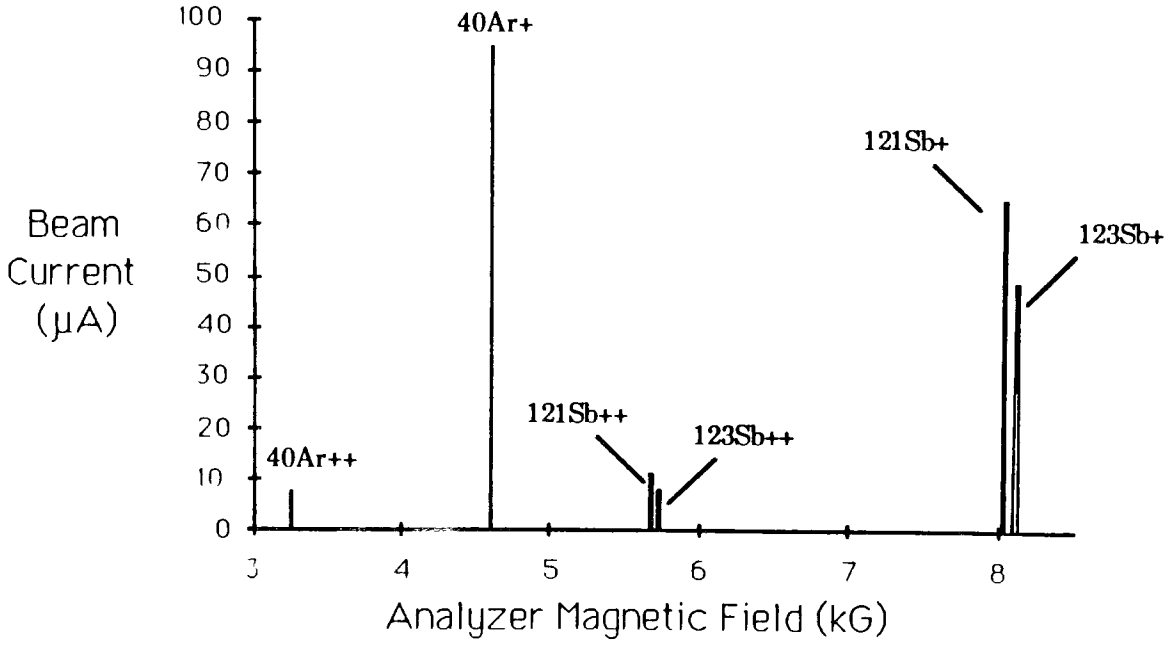


Figure 15

Sb Beam Current vs. Energy

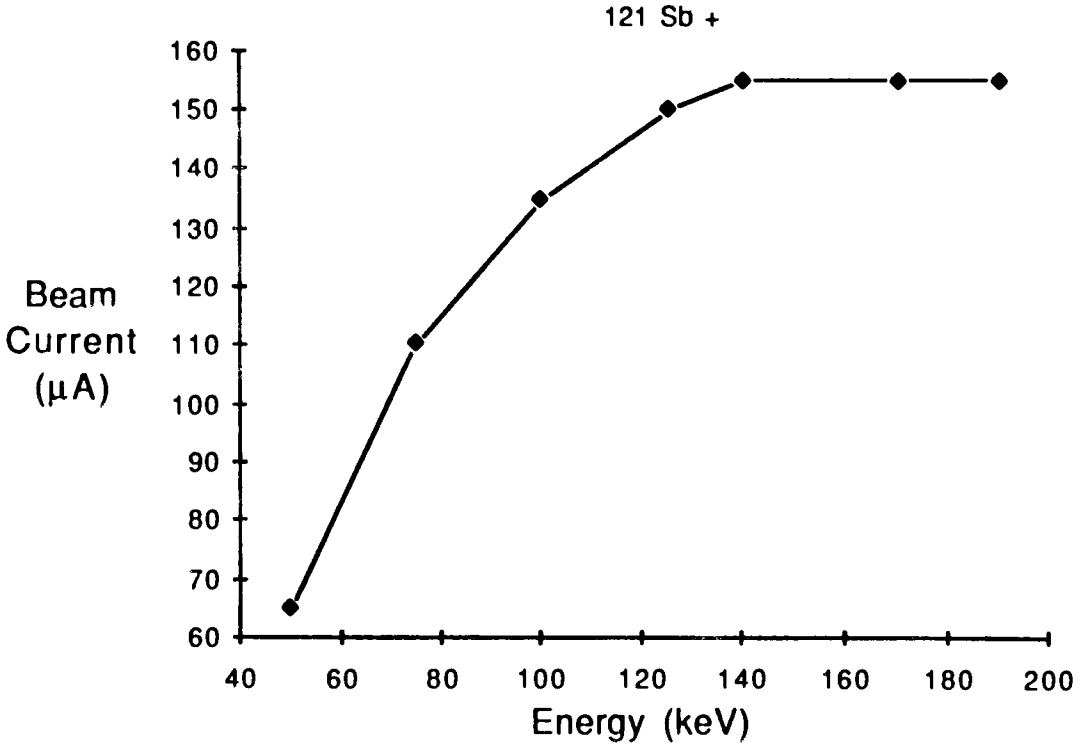


Figure 16

are then measured using SIMS. In Figure 17, profiles are shown for 100 keV and 190 keV implants into Si. The corresponding profiles in SiO_2 are shown in Figure 18. The values of R_p and ΔR_p determined from these profiles agree with the published data (see Figures 8 and 9) to within 15%. Additionally, the difference between the dose determined by integrating the concentration profile and the actual implanted dose is less than 25% in all cases.

Bare wafers are used for the isochronal RTA determination of $\emptyset_c$. For the sake of comparison, both $^{75}As^+$ and $^{121}Sb^+$ implants are studied. The implantation energy is chosen to be 50 keV since higher energies are expected to yield a more heavily damaged layer at a given dose. The doses range from $1 \times 10^{13}/cm^2$ to $1 \times 10^{15}/cm^2$.

Each implanted wafer is annealed for 60 seconds in N_2 at a temperature between 500°C and 850°C using a Tamarack 180 M incoherent lamp annealer. In this unit, radiant energy is directed upon the polished side of the wafer. An optical pyrometer measures the infrared energy emitted from the unpolished side of the wafer to

SIMS Profiles: Sb Implanted Into Si

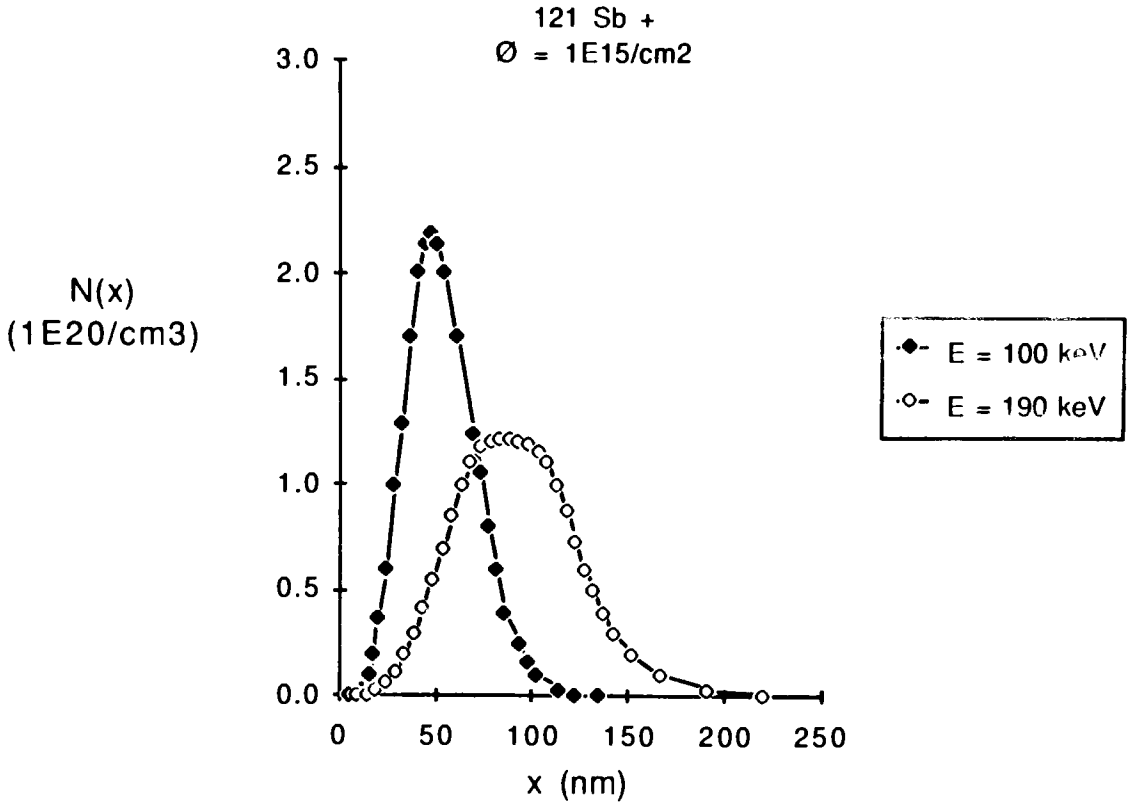


Figure 17

SIMS Profiles: Sb Implanted into SiO2

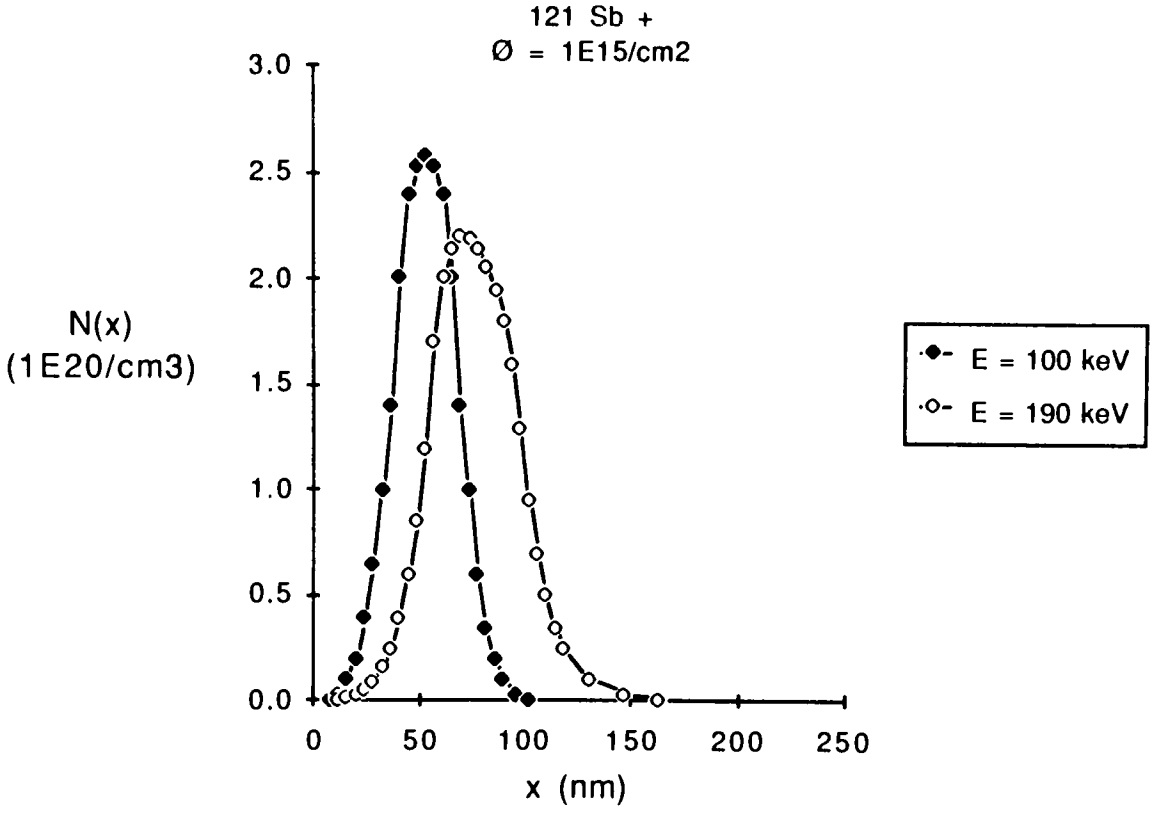


Figure 18

infer the temperature.

The sheet resistance of the of the annealed layers is measured with a four point probe. In Figure 19 the sheet resistance of As layers is plotted vs. RTA temperature, with implant dose as the parameter. The corresponding Sb data is plotted in Figure 20.

There are several interesting features common to Figures 19 and 20. For doses above a critical value, $\emptyset_c$, abrupt electrical activation of the dopant atoms occurs consistently at a relatively low temperature (about 575°C), while the activation increases marginally between 575°C and 850°C. For doses less than $\emptyset_c$, the increase in activation is more uniform with increasing temperature over the entire range.

The interpretation of $\emptyset_c$ as the dose necessary to form an amorphous surface layer in the Si is now discussed. If the implantation dose is such that a completely damaged surface layer is formed, then recrystalization during annealing can occur by solid phase epitaxy (SPE) from the underlying single crystal material. SPE, which occurs

Ion Implanted As Isochronal RTA Data

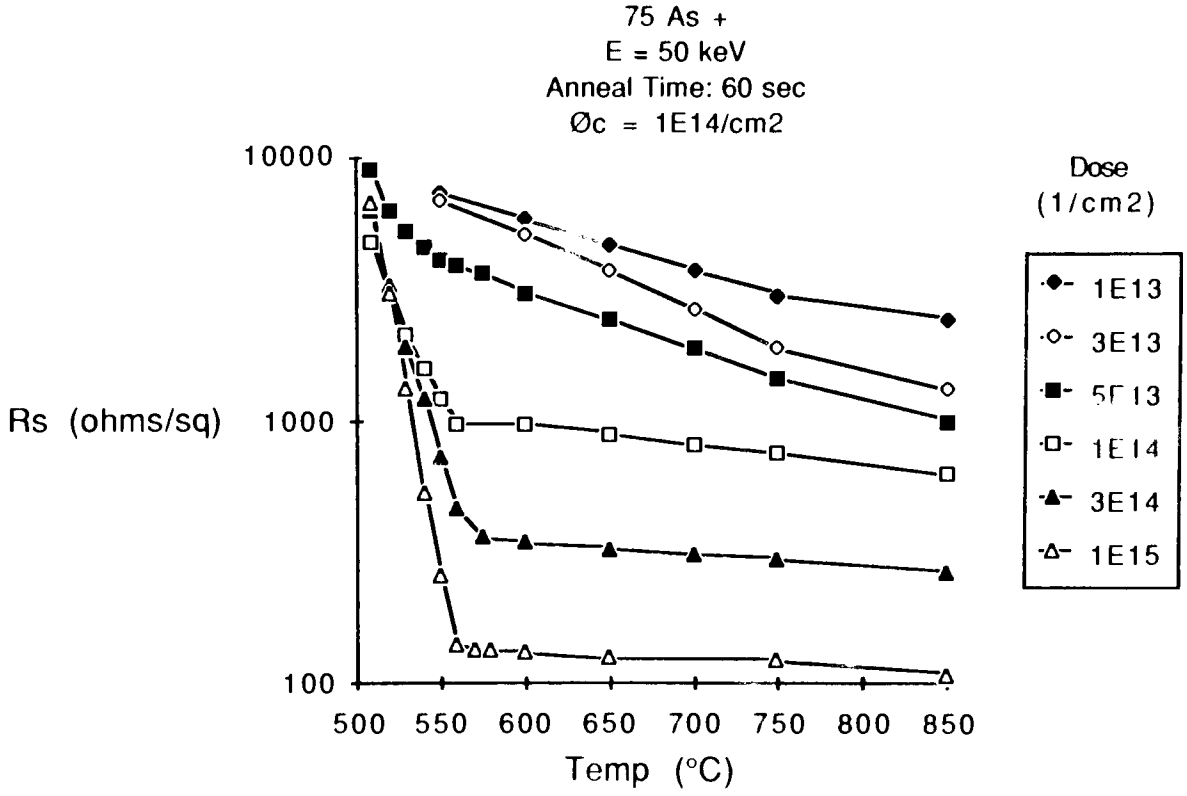


Figure 19

Ion Implanted Sb Isochronal RTA Data

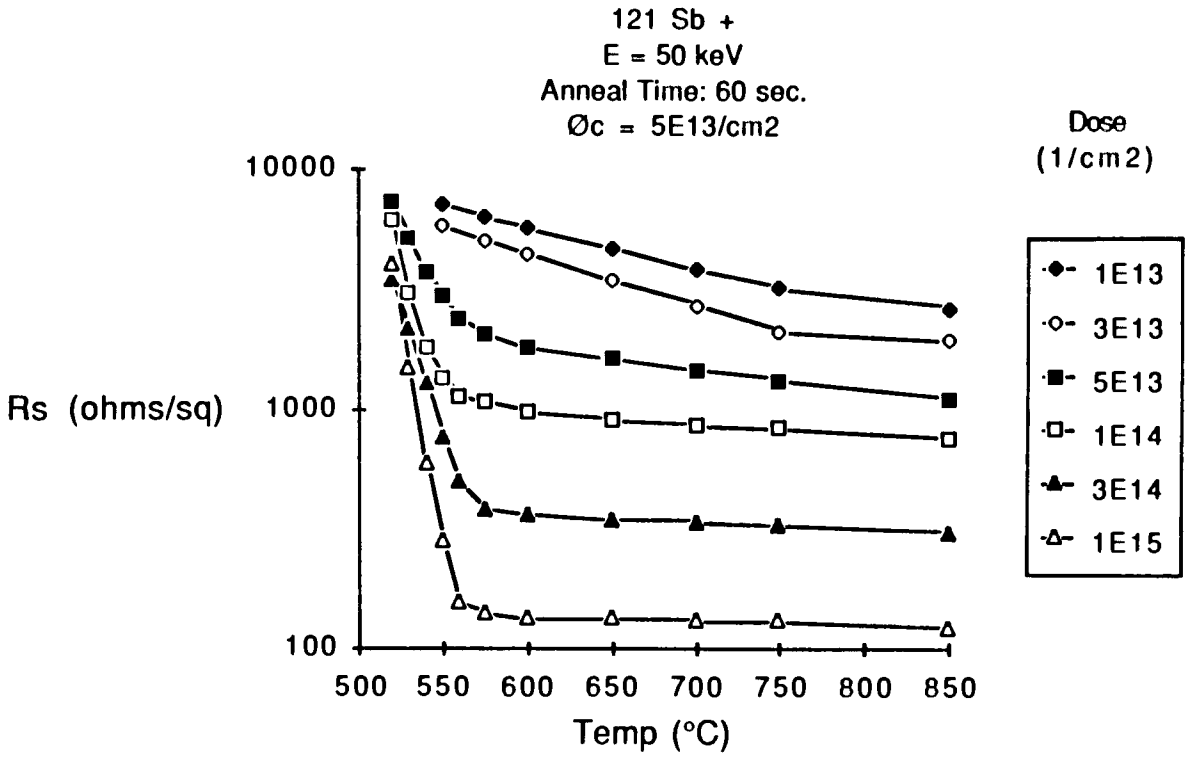


Figure 20

at temperatures as low as 550°C in Si, effectively activates implanted Group V donor atoms because they are vitually indistinguishable from neighboring Si atoms as far as the regrowth mechanism is concerned.[36] Lattice recrystallization and dopant incorporation proceed simultaneously from the undamaged interior region up to the wafer surface.

If the dose is below $\emptyset_c$, the implantation damage is not sufficient to completely destroy the lattice. Repair of the damage and substitutional incorporation of the dopant atoms requires long range migration of Si vacancies and interstitials and therefore higher annealing temperatures than for SPE regrowth.[37]

From Figures 19 and 20, $1 \times 10^{14}/cm^2$ is identified as the value of $\emptyset_c$ for As while the corresponding value for Sb is $5 \times 10^{13}/cm^2$. These values are a factor of two less than previously published results for 40 keV implants and 30 minute furnace annealing.[38]

Wafers for the study of Sb ORD are initially cleaned and a 250 Å screen oxide layer is thermally grown. $^{121}Sb^+$ is implanted at

50 keV with doses between 2 x $10^{13}/cm^2$ and 1 x $10^{15}/cm^2$. The furnace diffusions, based on Version B targets, are conducted at 1200°C for two hours in either N_2 or dry O_2.

For the group diffused in dry O_2, the oxide thicknesses are measured on an ellipsometer to determine any variation with implant dose. As shown in Figure 21, there is a slight increase in oxidation rate for doses above $\emptyset_c$ (5 x $10^{13}/cm^2$). The total oxide thickness variation over the range of doses considered is less than 5%.

Four point probe measurements are then used to determine the sheet resistance of each Sb layer. The results, plotted in Figure 22, indicate a 10 to 20% increase in the sheet resistance of the O_2 diffused layers relative to the N_2 diffused layers.

Based on the Version B sheet resistance target value (< 400 Ω/□), the Sb concentration profiles of wafers that received a dose of 5 x$10^{13}/cm^2$ are measured using SRP. To determine any extrinsic

Oxide Thickness vs Sb Dose

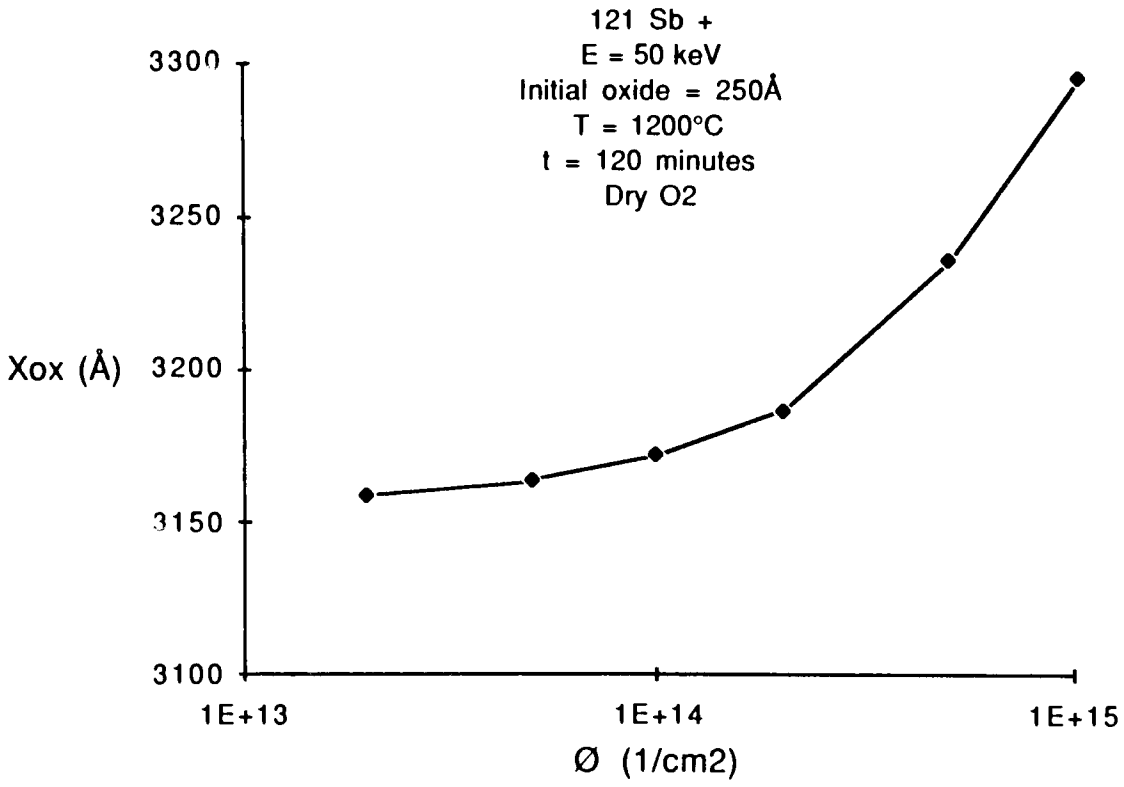


Figure 21

Sb ORD: Sheet Resistance vs Dose

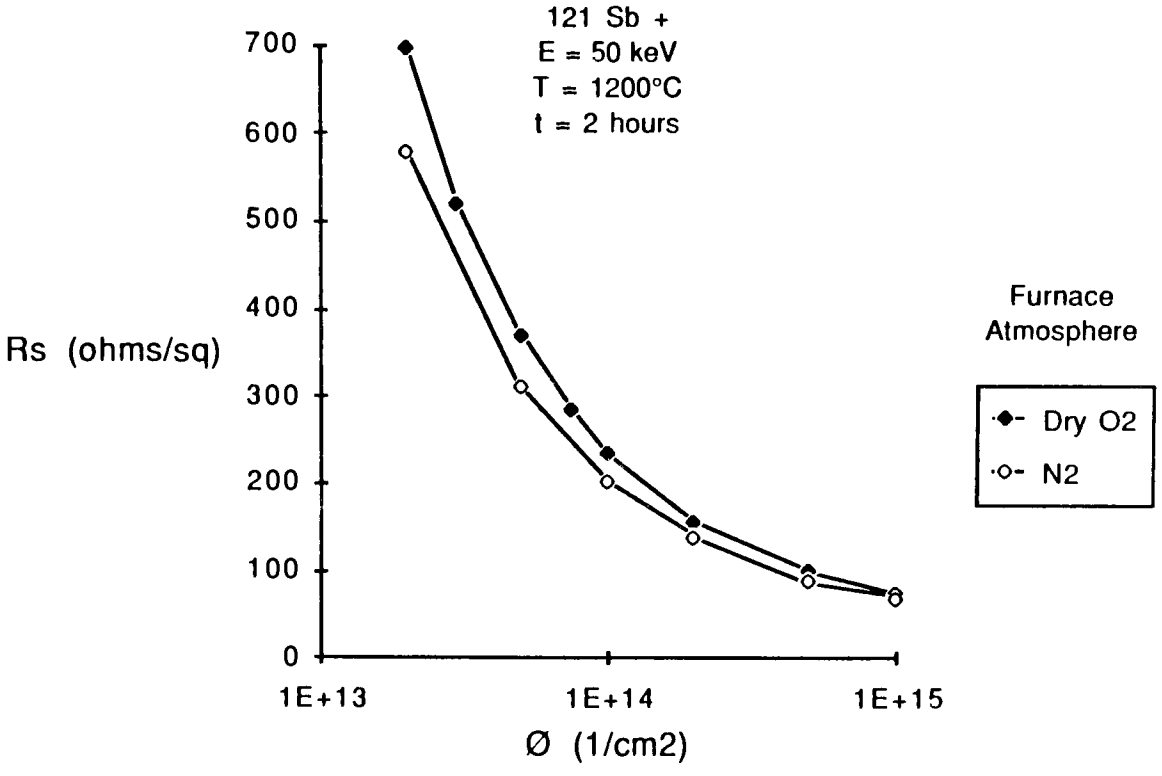


Figure 22

diffusion effects, SRP measurements are also performed on wafers that received a dose of $5 \times 10^{14}/cm^2$. The results are shown in Figures 23 and 24. It is clear that ORD causes about a 12% decrease in the junction depth of the Sb layers diffused in O_2 as compared with the layers diffused in N_2

SUPREM simulation of the Sb ORD results is executed by first using the default diffusion coefficients. SUPREM III[39] models the Sb diffusivity in a nonoxidizing atmosphere as the sum of two terms:

$$D_N(Sb) = D_i^0 + D_i^-(n/n_i) \qquad (5)$$

D_i^0 is the intrinsic diffusion coefficient associated with neutral charge state vacancy interactions and D_i^- is the intrinsic diffusion coefficient associated with singly charged negative vacancy interactions. The (n/n_i) factor accounts for changes in the charged vacancy concentration due to changes in the Fermi level.

Simulation of Sb diffusion in an oxidizing ambient is complicated by the recombination of vacancies with interstitials injected into the

Sb ORD: SRP Concentration Profiles

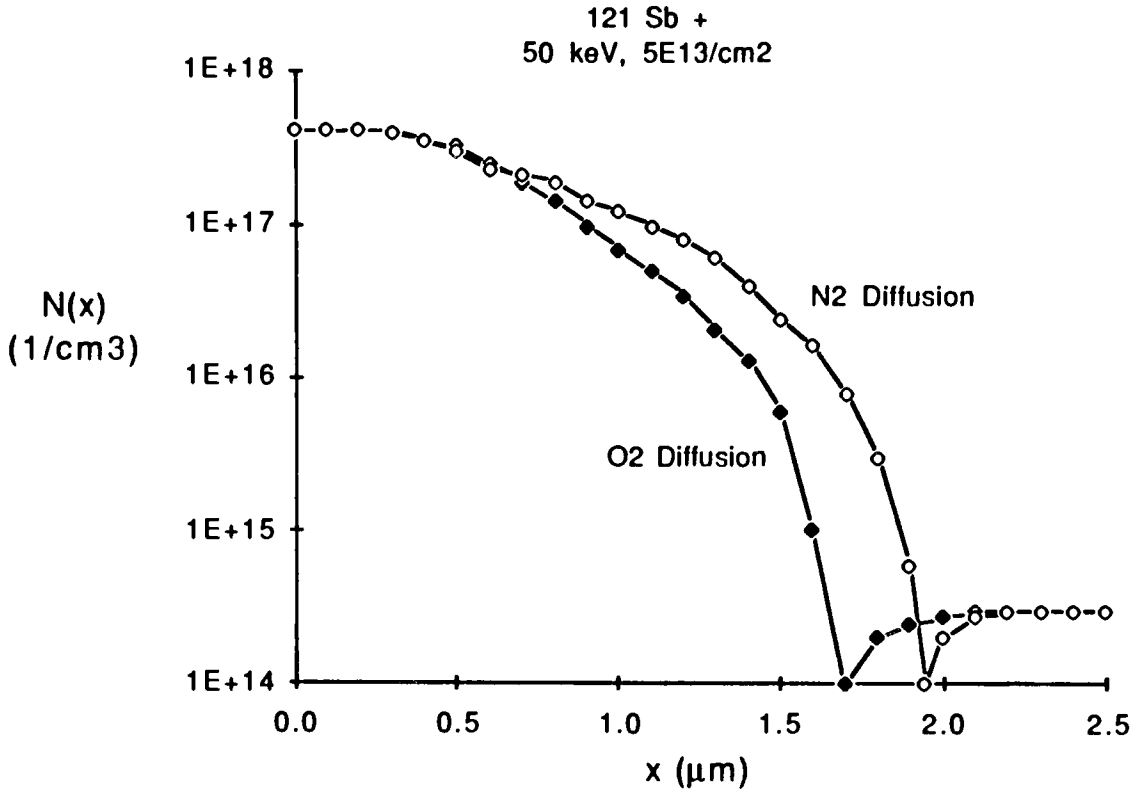


Figure 23

Sb ORD: SRP Concentration Profiles

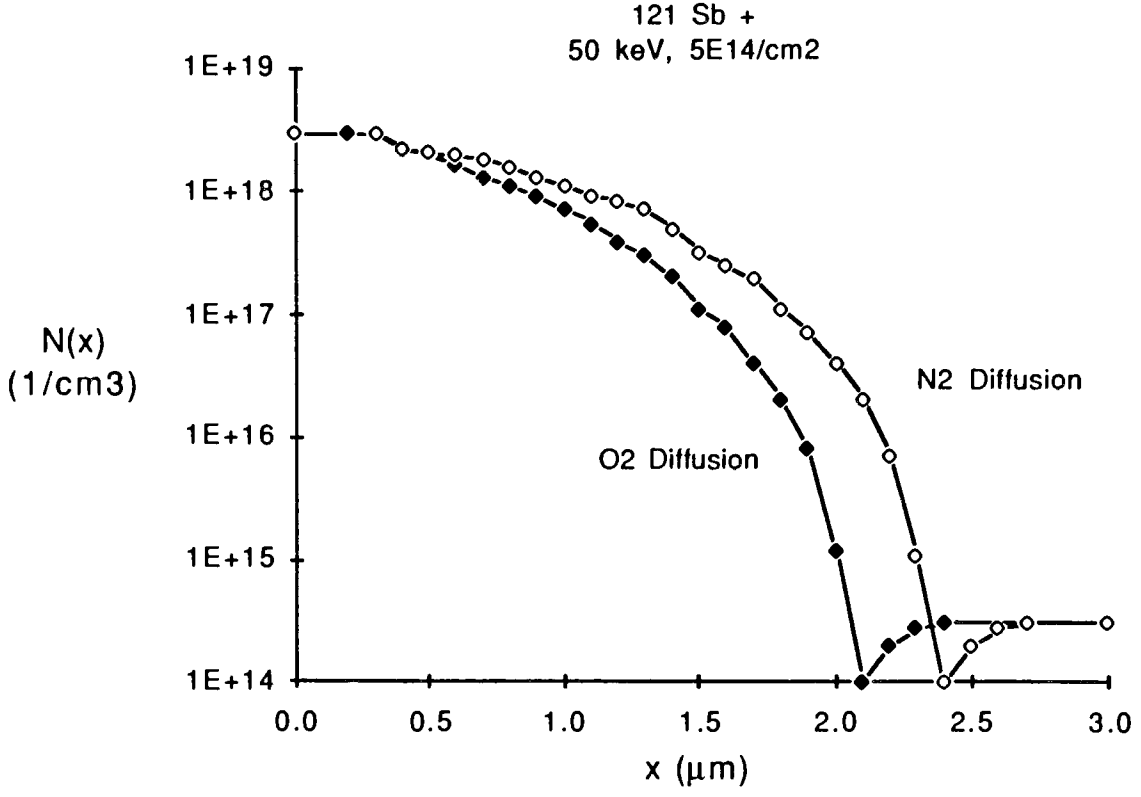


Figure 24

bulk from the oxidizing Si surface. The SUPREM III correction of the nonoxidizing Sb diffusivity to model ORD is of the form:

$$D(Sb) = D_N(Sb)[Si_I]_I/[Si_I] \qquad (6)$$

In the corrective factor, $[Si_I]_I$ is the concentration of interstitials in a nonoxidizing ambient and $[Si_I]$ is the concentration of interstitials in an oxidizing ambient.

Simulations of the ORD experiment, using the default values of the Sb diffusivity components, predict junction depths that are about 20% deeper than indicated by SRP and sheet resistances that are about 5 to 10% lower than the four point probe data. Simulated peak Sb concentrations are also overestimated by up to 140% relative to the SRP profiles. These errors occur for both N_2 and O_2 diffusions.

The depth accuracy of SRP[40] is within ± 3% and the absolute accuracy of the four point probe measurements* is within ± 2%. On the other

* National Bureau of Standards traceability for $R_s < 3000\ \Omega/\square$.

hand, the confidence level in the absolute carrier concentration values obtained from SRP profiles is not very high, particularly near the Si surface. Therefore, in adjusting the SUPREM parameters, the goal is to simulate correctly the junction depth and the sheet resistance of the Sb layers, while permitting the peak Sb concentration to vary.

The two intrinsic diffusion coefficients in equation (5) can each be expressed explicitly by an Arrhenius equation.[41] These equations along with their default values in SUPREM III are:

$$D_i^0 = D_0^0 \exp(-Q_i^0/k_BT)$$

$$= [(0.214)\exp(-3.65\ eV/k_BT)]\ cm^2/sec \qquad (7)$$

$$D_i^- = D_0^- \exp(-Q_i^-/k_BT)$$

$$= [(15.00)\exp(-4.08\ eV/k_BT)]\ cm^2/sec \qquad (8)$$

where k_B is the Boltzmann constant, 8.62×10^{-5} eV/°K and T is the temperature (in °K). If T = 1200°C (1473°K), then

$$D_i^0 = 7.02 \times 10^{-14}\ cm^2/sec$$

$$D_i^- = 1.66 \times 10^{-13}\ cm^2/sec$$

Since D_I^- is the dominant component of the Sb diffusivity at 1200°C, the pre-exponential term D_0^- should be modified to fit the SUPREM III model to the ORD experimental data. By trial and error, the default value is decreased until an acceptable fit is achieved. The value of D_0^- that yields an acceptable fit is 2/3 of the default value: D_0^-(modified) = 10 cm^2/sec. The experimental values of Sb layer junction depth, sheet resistance and peak concentration are listed in Table 4 along with the default and modified simulation results.

By virtue of the ORD and isochronal RTA studies, the annealing properties of ion implanted Sb in Si are sufficiently defined to continue with electrical characterization (R_s vs. Ø) for implant energies in excess of 50 keV. The maximum furnace temperature employed in the ORD study, 1200°C, is certainly an adequate drive-in temperature for both versions of the buried layer process. The higher energy values chosen are 90, 140 and 190 keV.*

*With V_x = 16 kV, the maximum energy of the CF4 is about 190 keV. The maximum beam current is realized if the energy is at least 140 keV. This defines an increment of 50 keV (and therefore 90 keV)

Table 4: Summary of Sb Oxidation Retarded Diffusion Stu-

Sb Layer Process Parameters		Junction Depth (μm)			Sheet Resistance (ohms/square)			Peak Concentration (atoms/cm3)		
Dose (ions/cm2)	Furnace Atmosphere	ED	SS-DEF	SS-MOD	ED	SS-DEF	SS-MOD	ED	SS-DEF	SS-MOD
5E13	O2	1.70	2.02	1.76	371.7	350.2	373.9	4.0E17	6.5E17	7.2E17
5E13	N2	1.95	2.38	2.10	309.4	295.8	312.5	4.5E17	6.0E17	6.5E17
5E14	O2	2.10	2.38	2.11	100.1	87.6	93.3	2.5E18	6.0E18	7.0E18
5E14	N2	2.40	2.79	2.47	85.9	76.0	80.3	3.0E18	5.3E18	6.0E18

Key to Abbreviations: ED ==> Experimental data

SS-DEF ==> SUPREM simulation results with default diffusion parameters

SS-MOD ==> SUPREM simulation results with modified diffusion parameter

Wafers for the higher energy Sb electrical characterization are initially cleaned and a 600 Å screen oxide layer is thermally grown. This oxide thickness is chosen to match the projected range of Sb at the intermediate energy (140 keV). $^{121}Sb^{+}$ is implanted over a range of doses (5×10^{14} to $6 \times 10^{15}/cm^2$) appropriate for the Version A sheet resistance target value (< 20 Ω/□).

In order to examine the role of any Sb atoms at or near the $Si-SiO_2$ interface, the wafers are split into two identical groups immediately following implantation. The screen oxide is removed from one group only. The two groups are then recombined and furnace annealed at 1200°C for eight hours in dry O_2.

The post-anneal oxide thicknesses of the wafers that retained the 600 Å screen oxide are evaluated to determine any dose dependence. The results, which indicate a 25% thickness variation over the range of doses considered (not including the Ø = 0 control), are shown in Figure 25.

Oxide Thickness vs Sb Dose

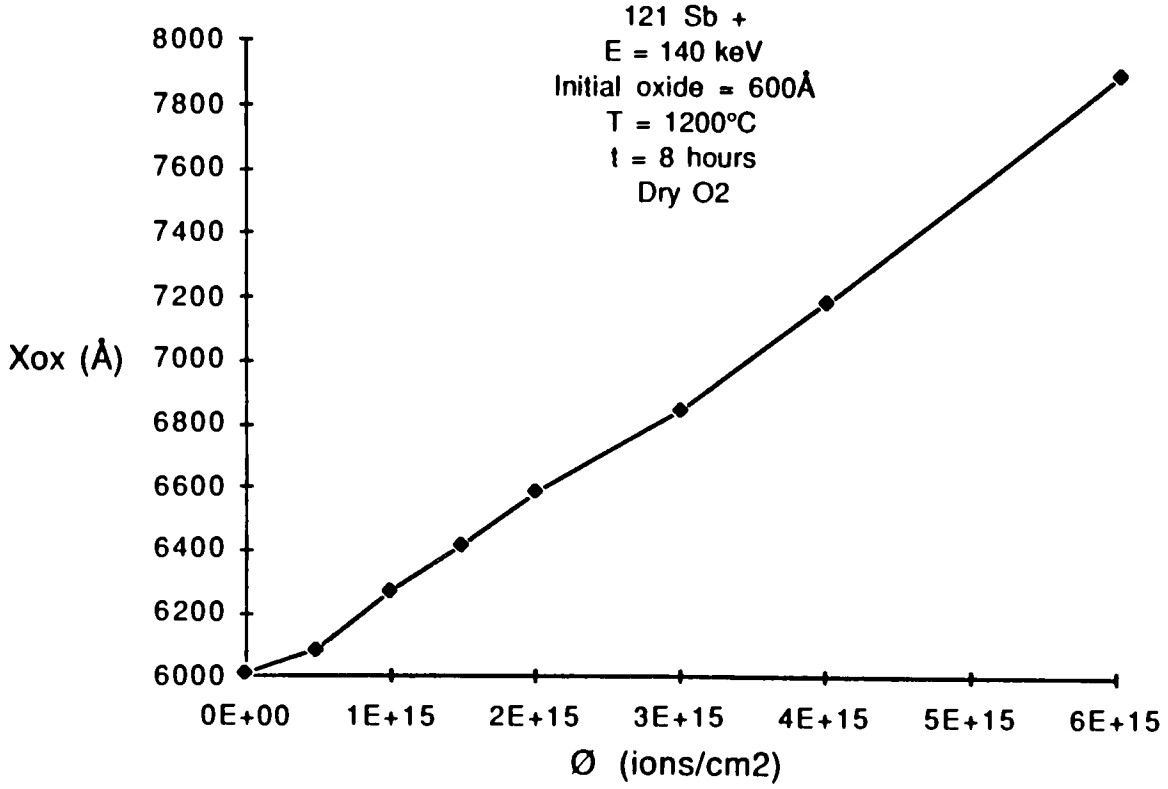


Figure 25

The sheet resistance of the each of the Sb layers is plotted vs. dose in Figures 26, 27 and 28 corresponding to implantation energies of 90, 140 and 190 keV, respectively. The curves are labeled with respect to the removal or retention of the screen oxide layer prior to diffusion. It is obvious that a significant amount of Sb is lost if the screen oxide is removed before diffusion. The degree of this loss is dependent upon the implantation energy. However, the energy dependence of the sheet resistance characteristic curves for the case of retained screen oxide is much less significant.

To investigate the mechanism of Sb loss, another group of wafers is similarly prepared for implantation. However, the screen oxide is removed from half of this group prior to implantation, ensuring that the total dose resides in the Si. The wafers are implanted with $^{121}Sb^{+}$ at 90 keV* and the same range of doses as the preceding experiment and are annealed under the same conditions.

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* The choice of 90 keV should maximize any loss due to the evaporation of Sb into the furnace ambient because of its closer proximity to the wafer surface as implanted relative to the higher energy Sb profiles.

Sheet Resistance vs Dose After Drive-In

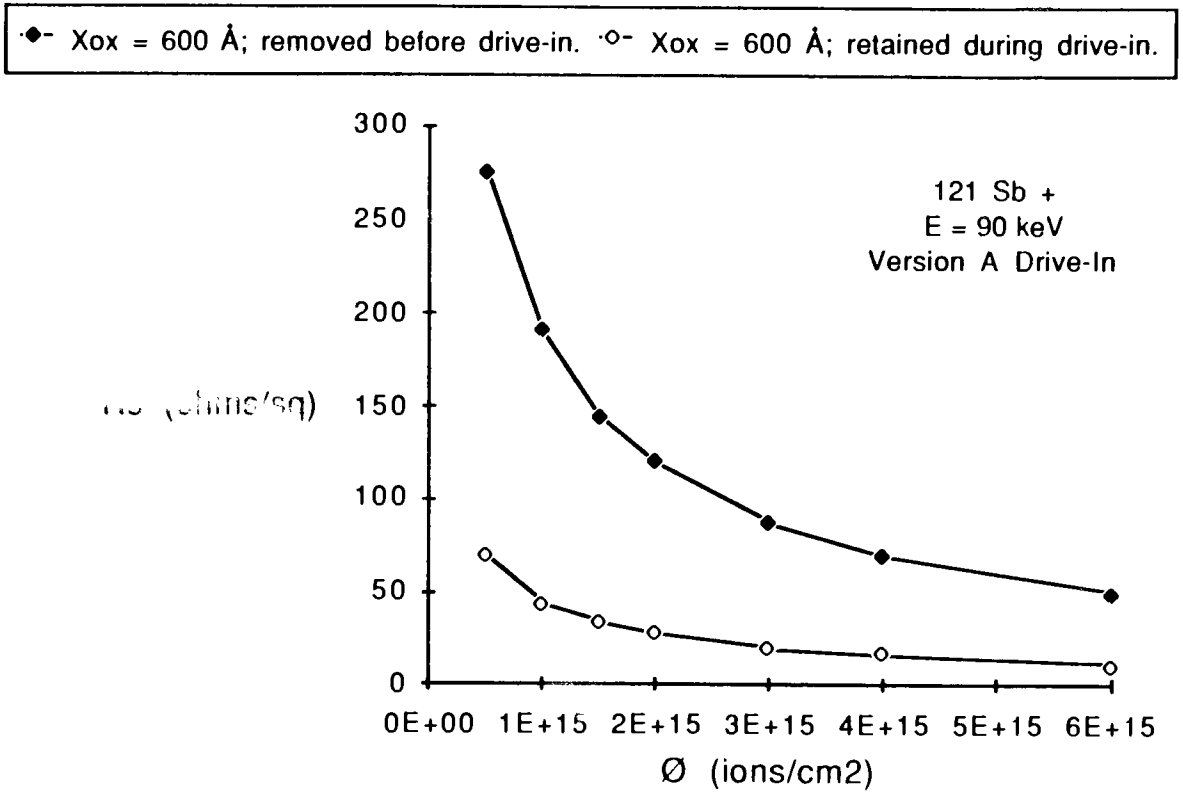


Figure 26

Sheet Resistance vs Dose After Drive-In

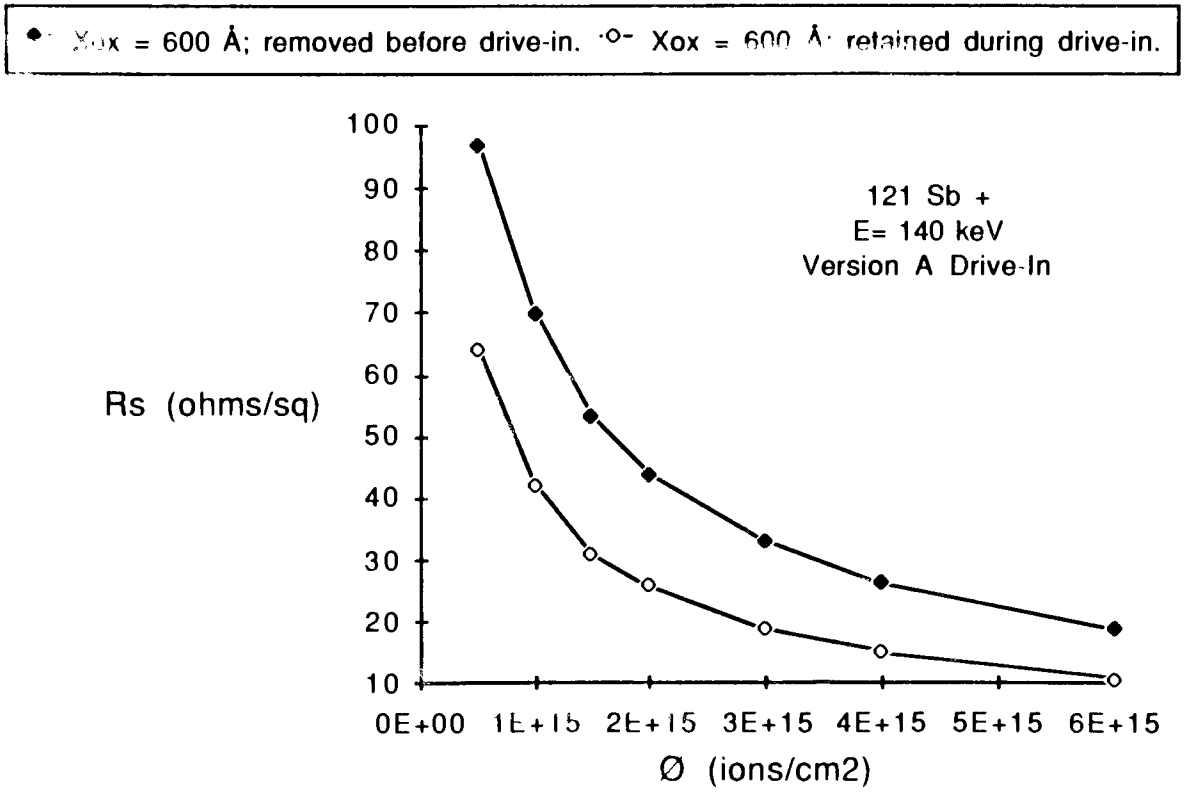


Figure 27

Sheet Resistance vs Dose After Drive-In

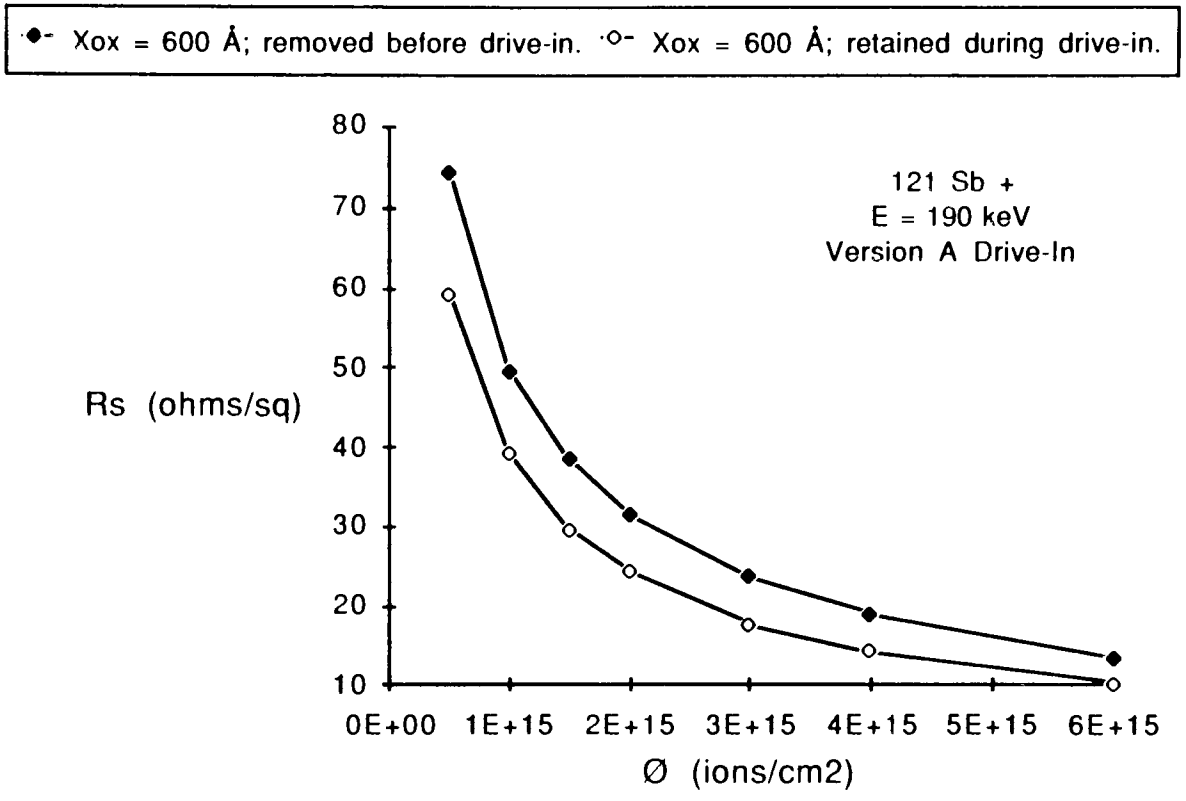


Figure 28

The resulting sheet resistance data for the "zero screen oxide" comparison is plotted in Figure 29. Note that the shift in sheet resistance values is only 10 to 20% as compared with the huge change (300 to 400%) induced by removal of the screen oxide after Sb implantation as shown in Figure 26. This suggests that a large fraction of the implanted Sb that is trapped in the screen oxide and/or at the Si-SiO_2 interface readily segregates into the Si during the annealing process.

Based on the Version A sheet resistance target value, the Sb concentration profile of the wafers that received a dose of $3 \times 10^{15}/cm^2$ and retained the screen oxide during diffusion are measured using SRP. The profiles for all three energy values are virtually identical. The profile of the wafer implanted at 190 keV is shown in Figure 30.

The characterization of ion implanted Sb is now at the point of process parameter specification. Based on the data obtained in the preceding experiments, parameters can be defined for both buried layer versions. With the exception of the junction depth, the Version

Sheet Resistance vs Dose: Zero Screen Oxide Comparison

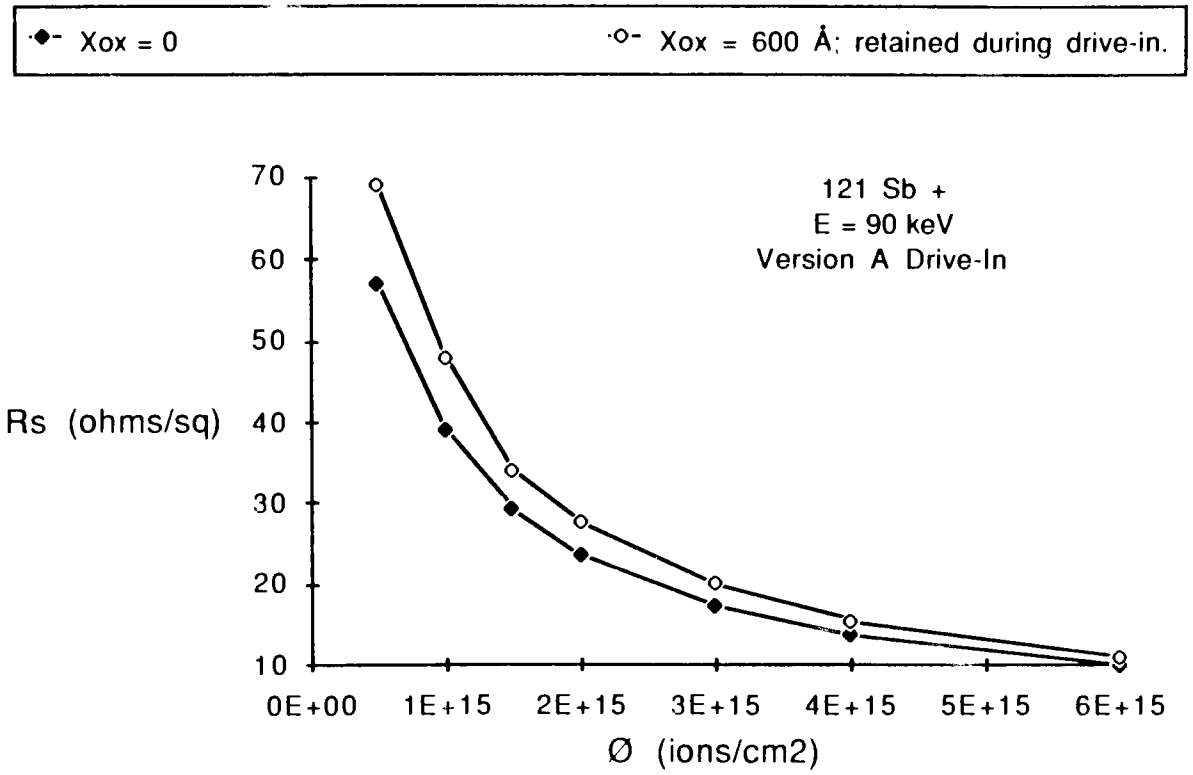


Figure 29

Sb: SRP Concentration Profile

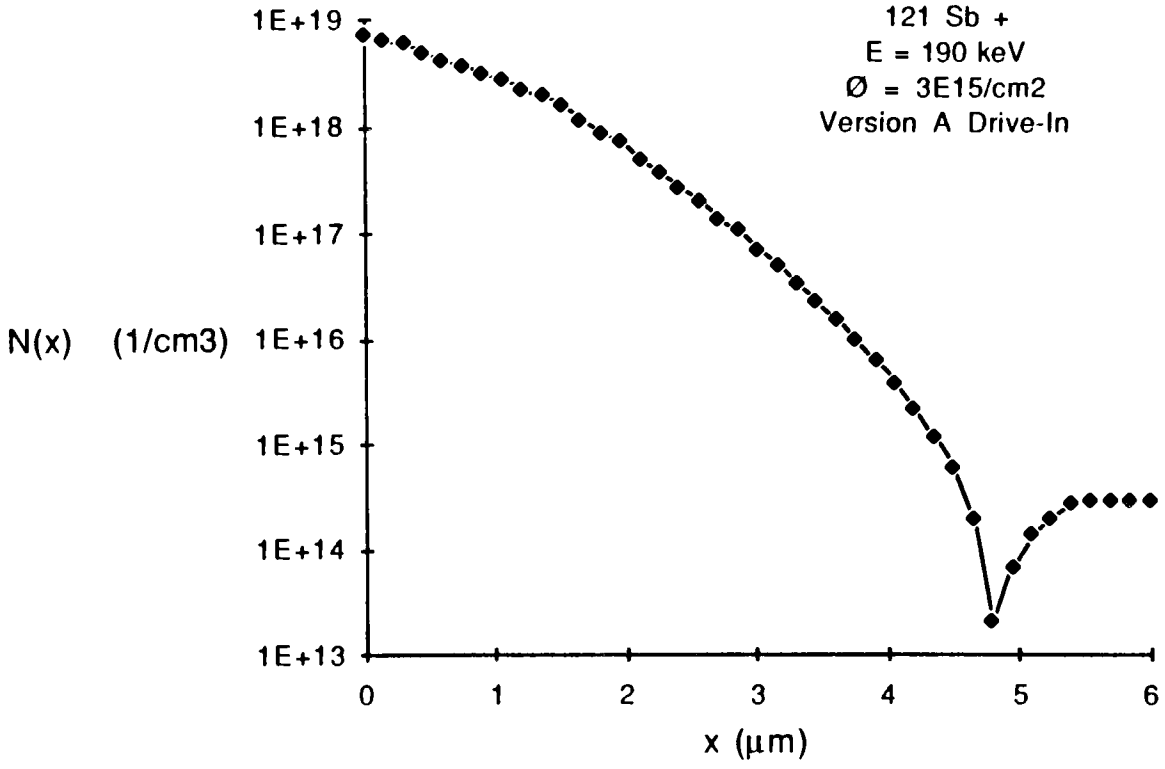


Figure 30

A targets are satisfied if $\emptyset \geq 3 \times 10^{15}$ cm^2 and E ≥ 90 keV. For maximum wafer throughput, 140 keV is chosen as the Version A energy (see Figure 16). With a similar exception in the junction depth, the Version B targets are satisfied if $\emptyset = 5 \times 10^{3}/cm^2$ and E = 50 keV.

Since the peak concentration and the sheet resistance are the two critical parameters of a buried layer, the specification of a junction depth target is intended only as a first order guideline. The fact that the measured junction depths are nearly 10% less than the original target values is of no real consequence.*

The complete listing of Sb buried layer process parameters is found in Table 5. Although no uniformity targets are explicitly defined for either version of the Sb process, sheet resistance contour maps are generated for many of the wafers processed in the preceding experiments. Typical maps of Version A and Version B layers are shown in Figures 31 and 32, respectively.

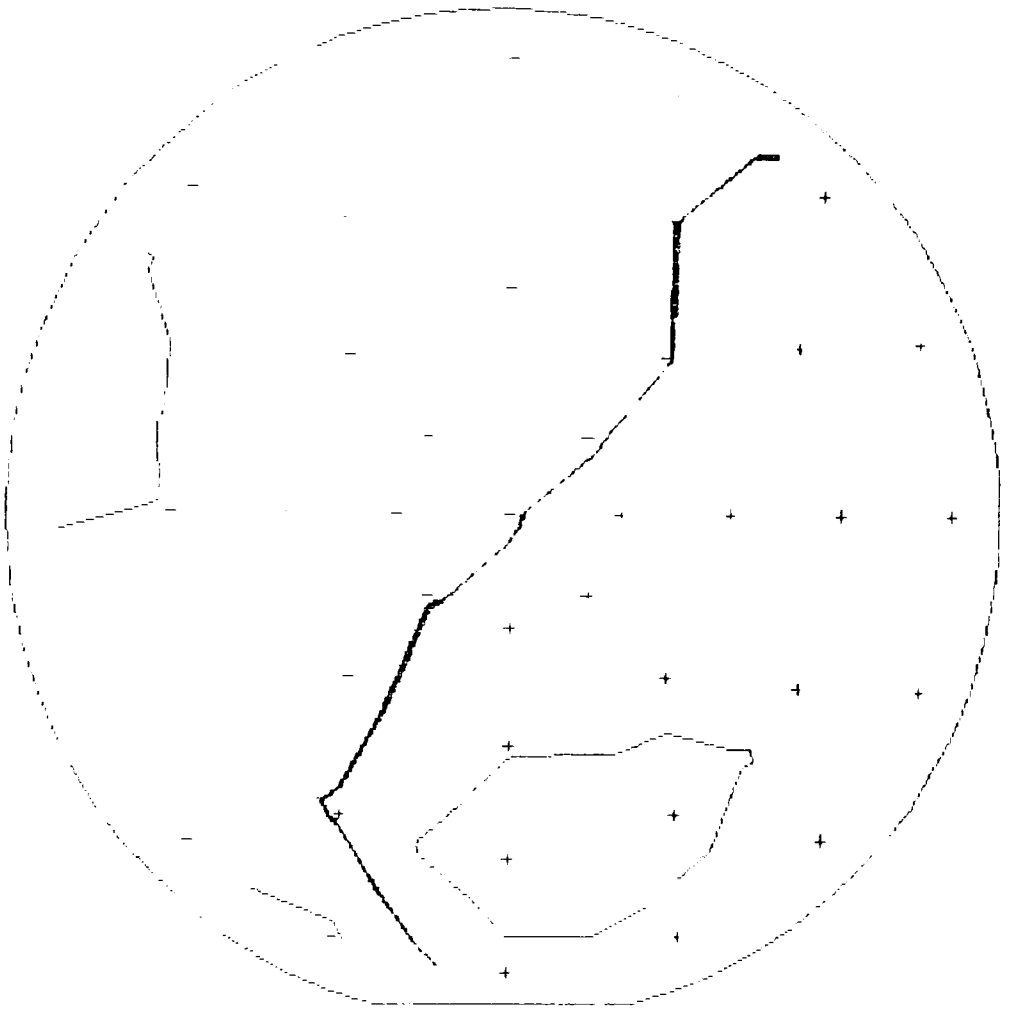
*The original target values were based upon preliminary SUPREM modeling which was conducted using the default Sb diffusivity.

Table 5: Summary of Ion Implanted Buried Layer Process Parameters

Process Parameter	Version A	Version B
Implantation Screen Oxide Thickness (Å)	600	250
Implantation Energy (keV)	140	50
Implantation Dose (ions/cm2)	3×10^{15}	5×10^{13}
Furnace Anneal Temperature (°C)	1200	1200
Anneal Time (hours)	8	2
Anneal Ambient	Dry Oxygen	Dry Oxygen

Version A Sheet Resistance Contour Map

121 Sb +
E = 140 keV, Ø = 3E15/cm2

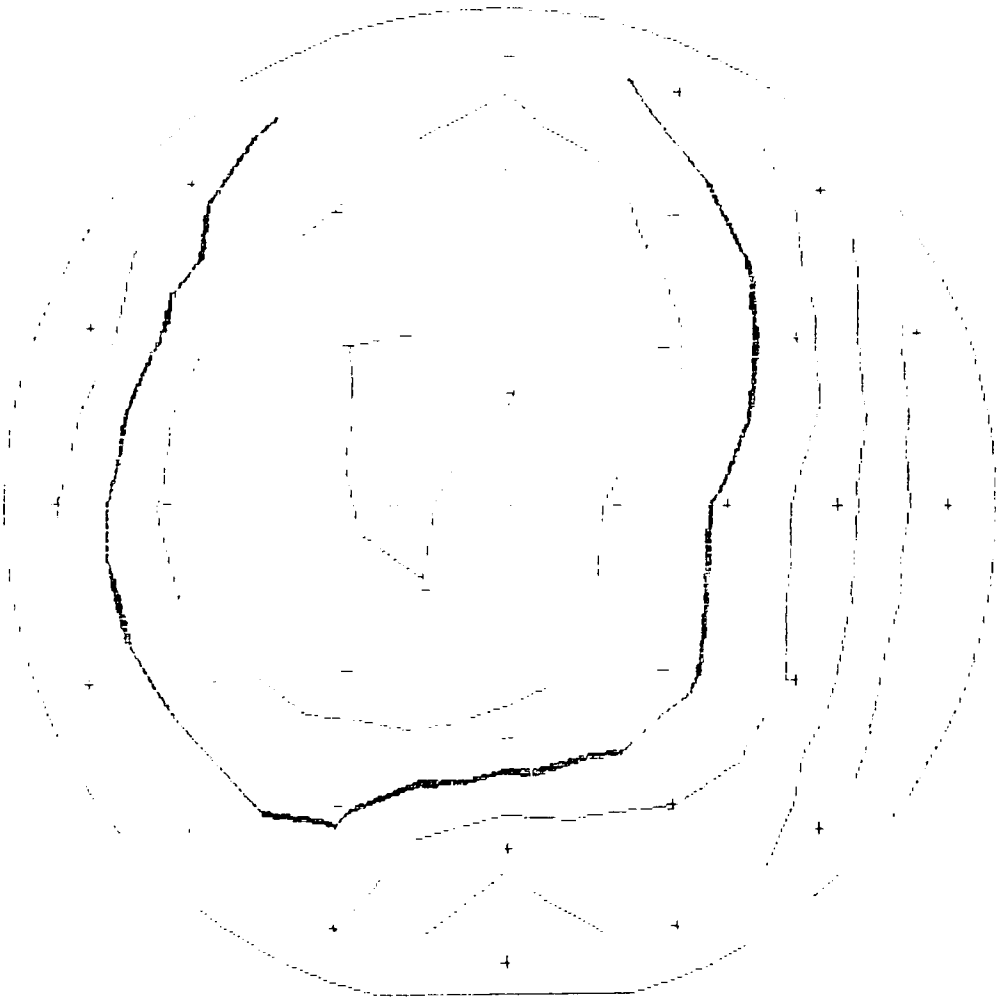


Average Sheet Resistance = 17.3 ohms/square (dark contour)
Standard Deviation = 0.07 ohms/square (0.4%)
Contour Interval: 0.09 ohms/square per contour (0.5%)

Figure 31

Version B Sheet Resistance Contour Map

121 Sb +
E = 50 keV, Ø = 5E13/cm2



Average Sheet Resistance = 371.7 ohms/square (dark contour)
Standard Deviation = 3.2 ohms/square (0.85%)
Contour Interval: 1.9 ohms/square per contour (0.5%)

Figure 32

The Version B Sb process is selected for an autodoping evaluation since a minimal transition width from the buried layer to the epi-layer is required. Wafers are initially cleaned and oxidized (600 Å) prior to ion implantation. Half of the wafers are implanted with $^{121}Sb^{+}$ and the others are implanted with $^{75}As^{+}$ with the same energy and dose (50 keV, 5 x $10^{15}/cm^2$). SRP is used to verify that the As concentration profile after diffusion is similar to that of Sb; see Figure 33.

A 2 µm thick p-type epi-layer is deposited on both sets of wafers. A reduced pressure (80 torr) deposition process is used for the As doped wafers while an atmospheric pressure process is used for the Sb doped wafers. The concentration profiles of the resulting As and Sb buried layer structures, again obtained using SRP, are shown in Figures 34 and 35, respectively.

The buried layer profiles indicate virtually no difference in the epi-layer to buried layer transition width or the homogeneously doped epi-layer thickness. The need for reduced pressure epitaxy is therefore eliminated if Sb is substituted for As. However, the

As: SRP Concentration Profile

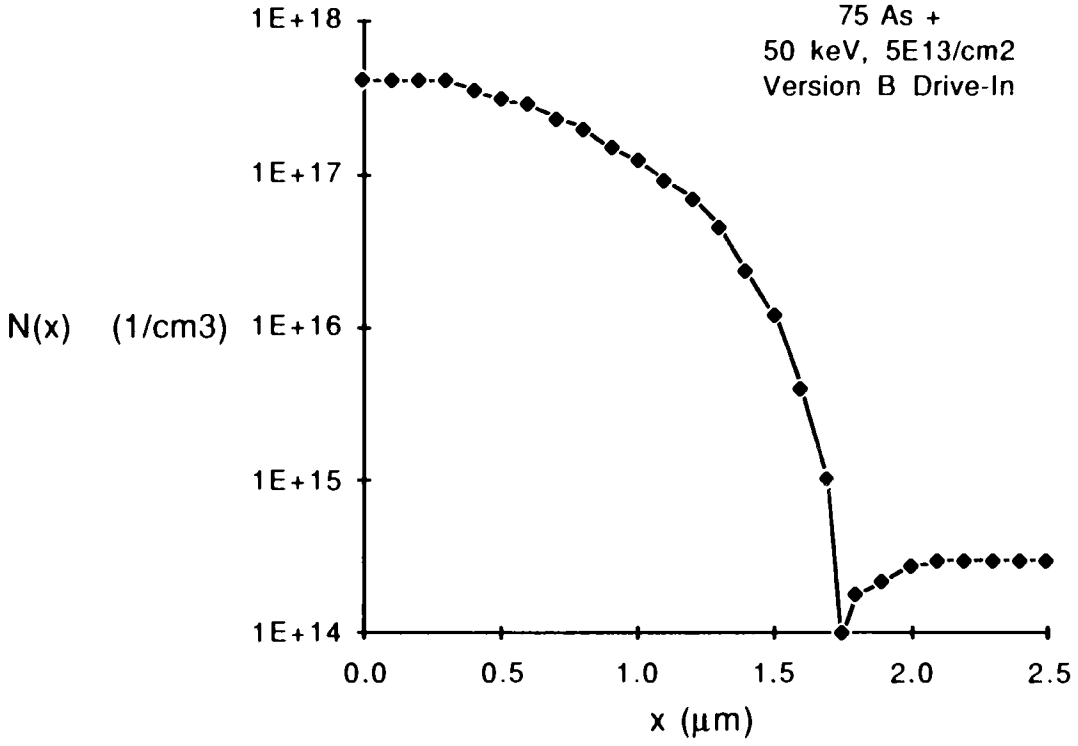


Figure 33

As Version B Buried Layer SRP Profile

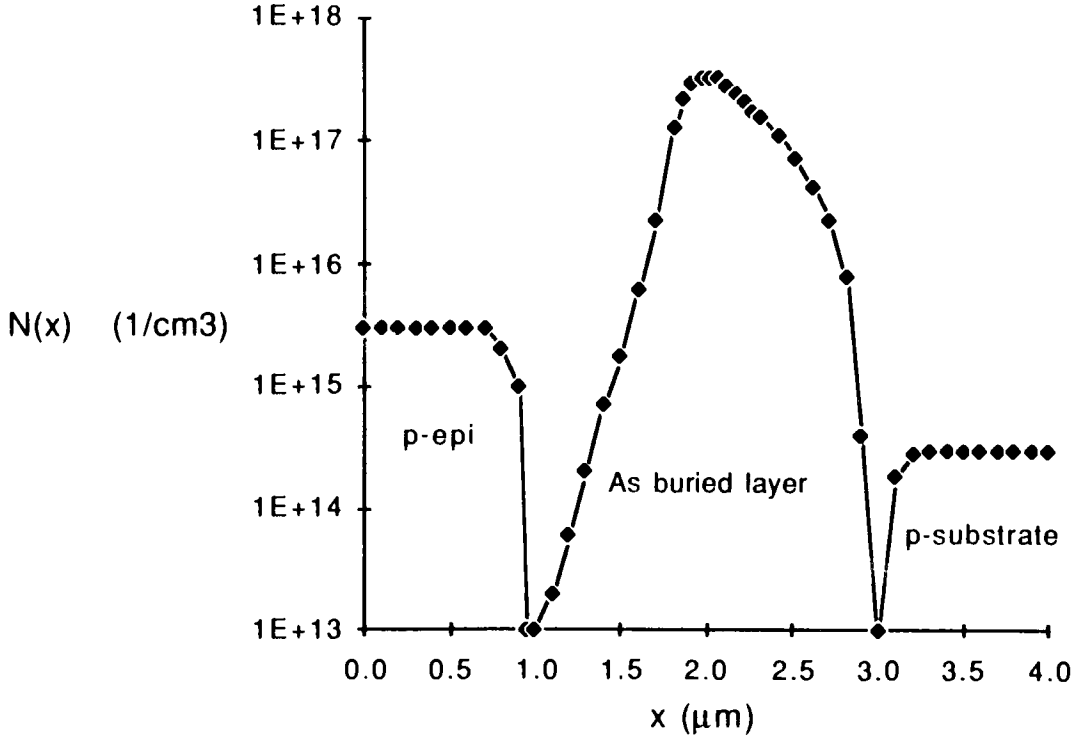


Figure 34

Sb Version B Buried Layer SRP Profile

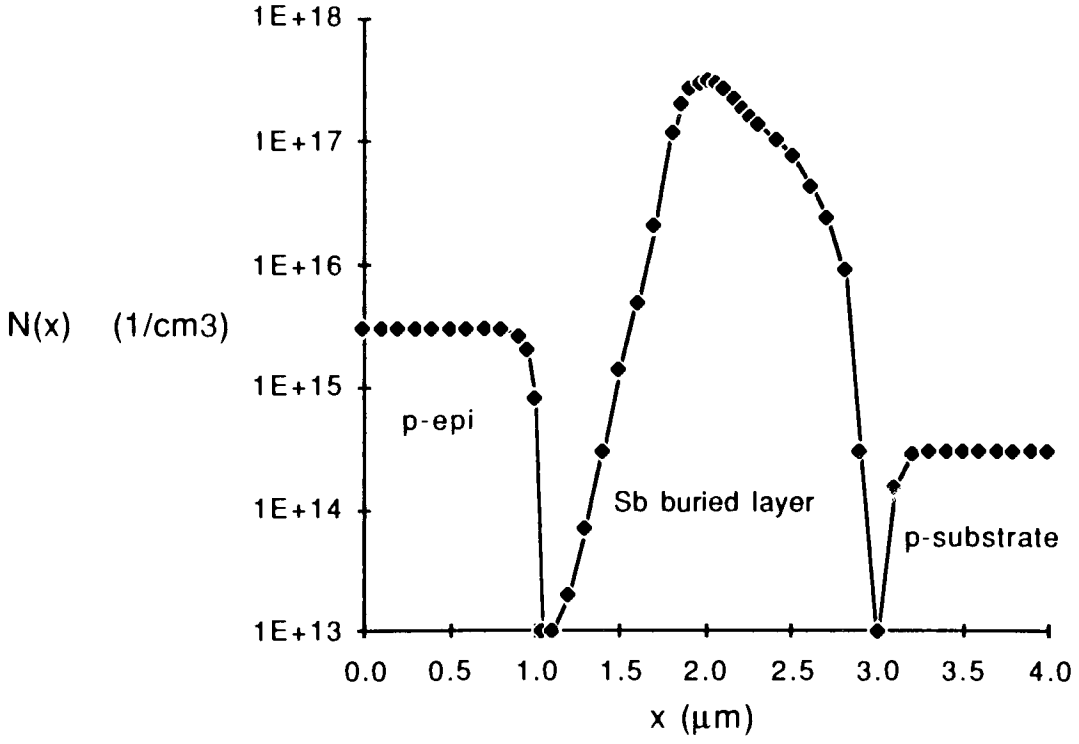


Figure 35

combination of reduced pressure epitaxy and Sb buried layers can be useful in the control of pattern washout and distortion.[42] Rather than relying upon the epi-reactor pressure to reduce autodoping (as is necessary with As buried layers), it is available as an extra degree of freedom in the deposition process to preserve any steps on the surface of the Si substrate.

VI. SUMMARY

Ion implanted $^{121}Sb^{+}$ was characterized as an n-type dopant in Si. Fundamental properties such as the two moment range statistics and the critical dose for amorphization were determined at energies which were anticipated for eventual device applications. The oxidation retarded diffusion of Sb was quantified at a furnace temperature sufficient to realize typical buried layer junction depths.

Electrical characterization of implanted and diffused Sb layers was conducted over intermediate and high dose ranges as mandated by two distinct process applications. The effect of Sb dose on the oxidation rate of Si was also determined in the same dose ranges Process parameters have been specified for both applications.

Finally, a comparative study of Sb and As was used to establish the suitability of Sb as a buried layer dopant with an atmospheric pressure epi-layer deposition process.

REFERENCES:

1. H. Frauenfelder and E. Henley, Nuclear and Particle Physics A: Background and Symmetries, pp. 8-9, Benjamin, Reading, Mass., 1975.

2. J. F. Ziegler, "Ion Implantation Science and Technology," p. xi, Academic Press, Orlando, Florida, 1984.

3. J. Lindhard, M. Scharff and H. E. Schiott, "Range Concepts and Heavy Ion Ranges," Mat. Fys. Medd. Dan. Vid. Selsk., Vol. 33, No.14, pp. 1-42, 1963.

4. J. B. Marion, Classical Dynamics of Particles and Systems, Second edition, pp. 292-298, Academic, New York, 1970.

5. T. E. Seidel, "Ion Implantation," in VLSI Technology, pp. 224-233, edited by S. M. Sze, McGraw Hill, New York, 1983.

6. S. Selberherr, Analysis and Simulation of Semiconductor Devices, pp. 46-62, Springer-Verlag/Wien, New York, 1984.

7. Varian/Extrion DF4/CF4 specification booklet, p. 3; specs. for 4 inch wafers.

8. Varian SEG DF4/DF3000 Operator's Course Instruction Guide Chapter 1, 1983.

9. R. A. Moline, R. Lieberman, J. Simpson and A. U. MacRae,"The Growth of High Quality Epitaxial Silicon Over Ion Implanted Buried Arsenic Layers," Journal of the Electrochemical Society, Vol. 121, pp. 1362-1366, October, 1974.

10. G. M. Oleszek, D. Metzger and K. L. Kasley, "Sb Implantation for Bipolar Buried Layers Using SbF_5 in a Cold Cathode Implantation System," Nuclear Instruments and Methods in Physics Research, Vol. B6, pp. 389-393, 1985.

11. W. K. Chu, R. H. Kastl and P. C. Murley, "Low Energy Antimony Implantation in Silicon: I. Profile Measurements and Calculation," Radiation Effects, Vol. 47, pp. 1-6, 1980.

12. E. Guerrero, H. Potzl, G. Stingeder, M. Grasserbauer, K. Piplitz and W. K. Chu, "Annealing of High Dose Sb-Implanted Single Crystal Silicon," Journal of the Electrochemical Society, pp. 3048-3052, December, 1985.

13. G. A. Sai-Halasz, K. T. Short and J. S. Williams, "Antimony and Arsenic Segregation at $Si-SiO_2$ Interfaces," IEEE Electron Device Letters, Vol. EDL-6, No. 6, pp. 285-287, June, 1985.

14. A. Nylandsted Larsen, F. T. Pederson, G. Weyer, R. Galloni, R. Rizzoli and A. Armigliato, "The Nature of Electrically Inactive Antimony in Silicon," Journal of Applied Physics, Vol. 59, No.6, pp.1908-1917, 15 March, 1986.

15. S. Mizuo and H. Higuchi, "Retardation of Sb Diffusion in Si During Thermal Oxidation," Japanese Journal of Applied Physics, Vol. 20, No. 4, pp. 739-744, April, 1981.

16. A. B. Glaser and G. E. Subak-Sharpe, Integrated Circuit Engineering, p. 254, Addison-Wesley, Reading, Mass., 1979.

17. J. O. Borland and T. Deacon, "Advanced CMOS Epitaxial Processing for Latch-Up Hardening and Improved Epilayer Quality," Solid State Technology, Vol. 27, No. 8, pp. 123-131, August, 1984.

18. J. P. Gailliard, M. Dupuy, M. Garcia, J. C. Roussin and M. Rouche, "High Dose Implantations of Antimony for Buried Layer Applications," Radiation Effects, Nol. 47, pp. 131-136, 1980.

19. G. A. Rozgonyi, R. P. Deysher and C. W. Pearce, "The Identification, Annihilation, and Suppression of Nucleation Sites Responsible for Silicon Epitaxial Stacking Faults," Journal of the Electrochemical Society, Vol. 123, No. 12, pp. 1910-1915, December, 1976.

20. M. L. Hammond, "Silicon Epitaxy," Solid State Technology, Vol. 21, No. 11, pp. 68-75, November, 1978.

21. A. Schmitt and G. Schorer, "Damage Anneal of Antimony/Phosphorus Double Implants in Silicon," Applied Physics, Vol. 22, pp. 137-143, 1980.

22. S. Ogura, P. J. Tsang, W. W. Walker, D. L. Critchlow and J. F. Shepard, "Design and Characteristics of the LDD IGFET," IEEE Transactions on Electron Devices, Vol. ED-27, pp. 1359-1367, August, 1980

23. P. J. Tsang, S. Ogura, W. W. Walker, J. F. Shepard and D. L. Critchlow, "Fabrication of High-Performance LDDFETs with Oxide Sidewall Spacer Technology," IEEE Transactions on Electron Devices, Vol. ED-29, pp. 590-596, April, 1982.

24. G. A. Sai-Halasz, "Implant-Defined Shallow FET Source/Drain Junctions," IBM Technical Disclosure Bulletin, Vol. 26, pp. 3018-3019, 1983.

25. G. A. Sai-Halasz and H. B. Harrison, "Device-Grade Ultra-Shallow Junctions Fabricated with Antimony," IEEE Electron Device Letters, Vol. EDL-7, No. 9, pp. 534-536, September, 1986.

26. W. K. Chu, M. J. Sullivan, S. M. Ku and M. Shatzkes, "Low Energy Antimony Implantation in Silicon: II. Applications to Schottky Barrier Diode Adjustment and to Ion-Implanted Resistors," Radiation Effects, Vol. 47, pp. 7-14, 1980.

27. S. Ashok and B. J. Baliga, "Effect of Antimony Ion Implantation on Al-Silicon Schottky Diode Characteristics," Journal of Applied Physics, Vol. 56, No. 4, pp. 1237-1239, 15 August, 1984.

28. American Institute of Physics Handbook, Second edition, Section 7, p. 10, McGraw-Hill, New York, 1963.

29. J. C. Irvin, "Resistivity of Bulk Silicon and of Diffused Layers in Silicon," Bell System Technical Journal, Vol. XLI, No. 2, pp. 387-410, March, 1962.

30. B. L. Crowder and F. F. Morehead, Jr., "Annealing Characteristics of n-Type Dopants in Ion Implanted Silicon," Applied Physics Letters, Vol. 14, No. 10, pp. 313-315, 15 May, 1969.

31. C. P Ho, J. D. Plummer, S. E. Hansen and R. W. Dutton, "VLSI Process Modeling - SUPREM III," IEEE Transactions on Electron Devices, pp. 1438-1453, Vol. ED-30, No. 11, November, 1983.

32. R. A. Colclaser, Microelectronics: Processing and Device Design, pp. 144-146, Wiley, New York, 1980.

33. R. B. Herring, "Advances in Reduced Pressure Silicon Epitaxy," Solid State Technology, pp. 75-80, Vol. 22 No. 11, November, 1979.

34. Varian Extrion, "Waycool™ Installation and Maintenance Procedures," pp. 1-2.

35. J. L. Stone and J. C. Plunkett, "Ion Implantation Processes in Silicon," in Impurity Doping Processes in Silicon, pp. 83-87, edited by F. F. Y. Wang, North-Holland, Amsterdam 1981.

36. Reference 5, p. 244.

37. J. D. Plummer, Course Notes: "VLSI Devices and Technology," Section 27, pp. 5-10, Stanford University, 1985.

38. Reference 35, p. 84.

39. Reference 31, pp. 1442-1445.

40. Solecon Laboratories, SRP Accuracy Statement.

41. R. B. Fair, "Concentration Profiles of Diffused Dopants in Silicon," in Impurity Doping Processes in Silicon, p. 346, edited by F. F. Y. Wang, North-Holland, Amsterdam, 1981.

42. R. B. Herring, "Silicon Epitaxy at Reduced Pressure," Applied Materials Technical Report #HT-010, 1979.

APPENDIX 1: Derivation of the Mass Separation Relationship

The 90° band in the beamline of a CF4 ion implanter is nested within the field of the analyzer electromagnet. The motion of an ion of velocity v in a uniform magnet field B is determined by the magnetic term of the Lorentz force equation:

$$F = hq_e v \times B \tag{11}$$

where h is the charge state of the ion and q_e is the magnitude of the charge of an electron.

Referring to Figure 2, if the direction of the magnetic field is normal to the plane of the sketch and the direction of ion motion out of the source, then the vector relation reduces to scalar form:

$$F = hq_e vB \tag{11a}$$

The centripetal force necessary to bend the trajectory of ions of mass m into coincidence with the radius of curvature of the beamline, r, is

$$F_C = mv^2/r \tag{12}$$

Since the magnetic force must provide this centripetal force to ions

of the desired charge-to-mass ratio, we have

$$hq_e vB = mv^2/r \qquad (13)$$

If this is solved for v^2,

$$v^2 = (hq_e rB/m)^2 \qquad (13a)$$

The kinetic energy of the ions is

$$KE = mv^2/2 = hq_e V_x \qquad (14)$$

Again solving for v^2,

$$v^2 = 2hq_e V_x/m \qquad (14a)$$

Equating 13a and 14a, and solving for q_e/m, we obtain the result

$$q_e/m = 2V_x / (hr^2B^2) \qquad (2)$$

Ions extracted out of the source that do not satisfy this relationship collide with the walls of the 90° bend of the beamline.*

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*Ions with a charge-to-mass ratio greater than the right hand side of equation (2) collide with the inner surface of the bend (i.e. their trajectory is deflected too much by the magnetic force). Conversely, ions with a charge-to-mass ratio less than the right hand side of equation (2) collide with the outer surface of the bend.

APPENDIX 2:

Equipment:

1. Ion Implanter: Varian/Extrion Model 200-CF4
2. Solid Vaporizer: Varian/Extrion Model 200-20A2F
3. Rapid Thermal Annealer: Tamarack Scientific Model 180-M
4. Sheet Resistance Mapping System: Prometrix Model 111B

Materials:

1. Solid Sb Shot: Alfa Products Stock #800209